



4-STAGE DIVIDE-BY-8 JOHNSON COUNTER

The HEF4022B is a 4-stage divide-by-8 Johnson counter with eight spike-free decoded active HIGH outputs (O_0 to O_7), an active LOW output from the most significant flip-flop (\bar{O}_{4-7}), active HIGH and active LOW clock inputs (CP_0 , \overline{CP}_1) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW to HIGH transition at CP_0 while \overline{CP}_1 is LOW or a HIGH to LOW transition at \overline{CP}_1 while CP_0 is HIGH (see also function table). Either CP_0 or \overline{CP}_1 may be used as clock input to the counter and the other clock input may be used as a clock enable input. When cascading counters, the \bar{O}_{4-7} output, which is LOW while the counter is in states, 4, 5, 6 and 7, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($O_0 = \bar{O}_{4-7} = \text{HIGH}$; O_1 to $O_7 = \text{LOW}$) independent of the clock inputs (CP_0 , \overline{CP}_1).

Automatic code correction of the counter is provided by an internal circuit, following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

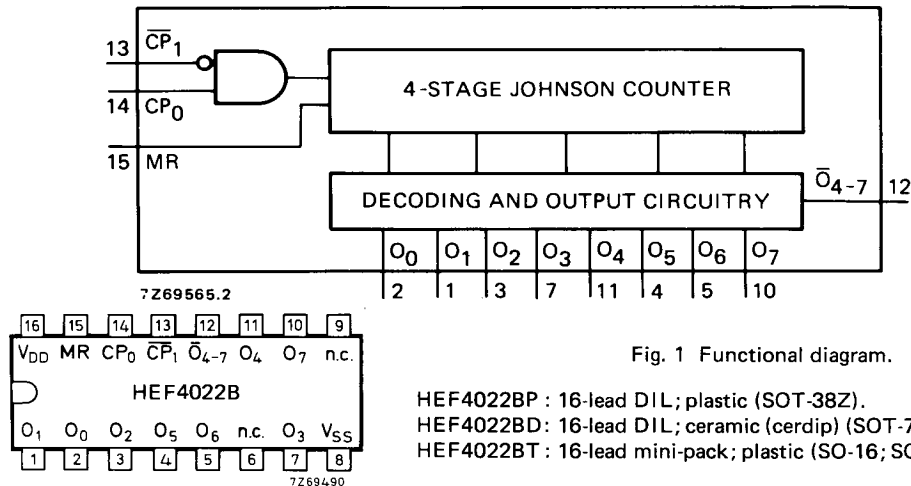


Fig. 1 Functional diagram.

HEF4022BP : 16-lead DIL; plastic (SOT-38Z).

HEF4022BD : 16-lead DIL; ceramic (cerdip) (SOT-74).

HEF4022BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

Fig. 2 Pinning diagram.

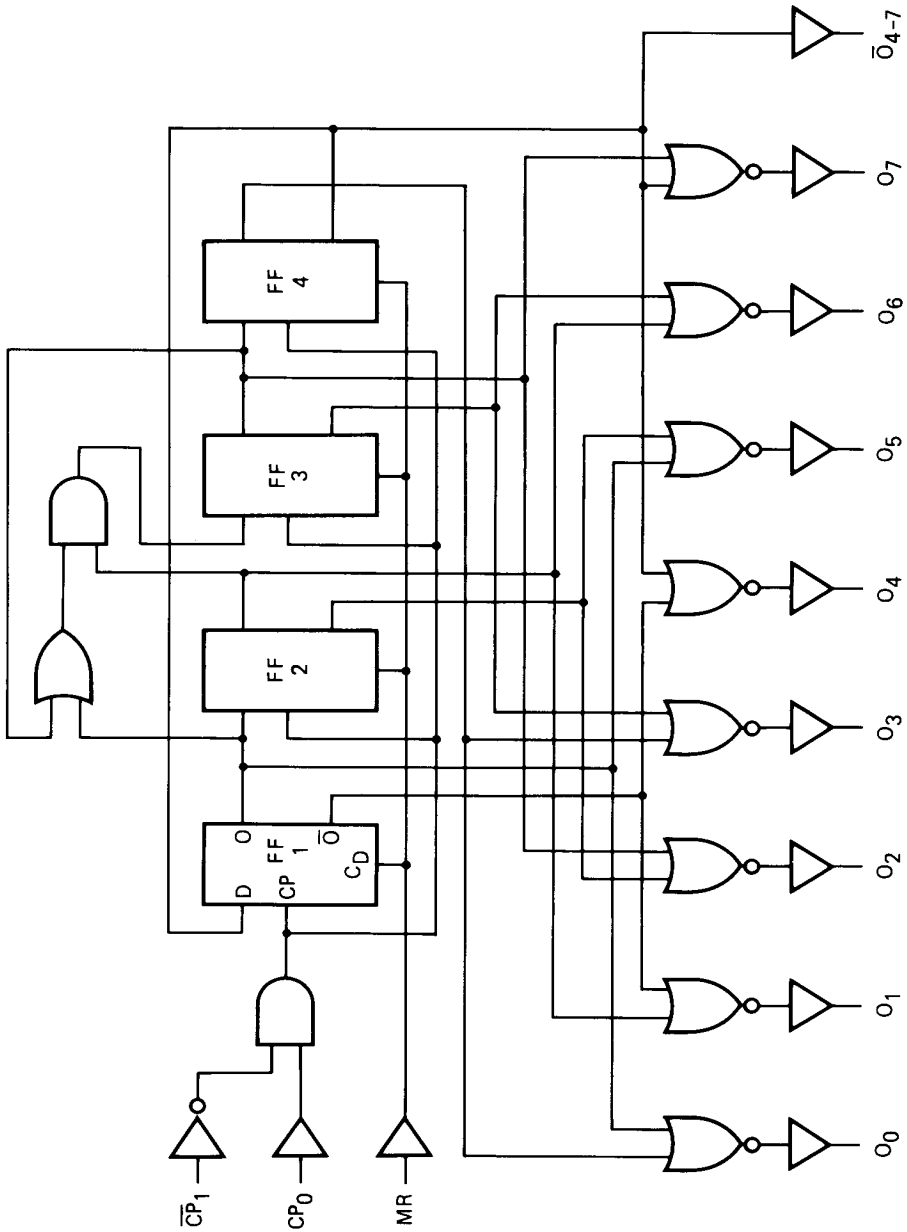
PINNING

CP_0	clock input (LOW to HIGH; edge-triggered)
\overline{CP}_1	clock input (HIGH to LOW; edge-triggered)
MR	master reset input
O_0 to O_7	decoded outputs
\bar{O}_{4-7}	carry output (active LOW)

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications



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Fig. 3 Logic diagram.

FUNCTION TABLE

MR	CP ₀	\overline{CP}_1	operation
H	X	X	$O_0 = \overline{O}_{4-7} = H$; O_1 to $O_7 = L$
L	H	\searrow	Counter advances
L	\swarrow	L	Counter advances
L	L	X	No change
L	X	H	No change
L	H	\swarrow	No change
L	\searrow	L	No change

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

 \swarrow = positive-going transition \searrow = negative-going transition

A.C. CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

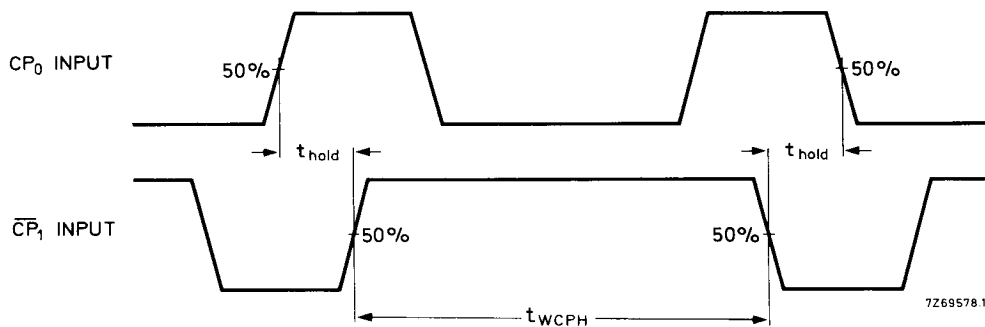
	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays $CP_0, \overline{CP}_1 \rightarrow O_n$ HIGH to LOW	5			195	390 ns	$168 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t _{PHL}		75	145 ns	$64 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			50	100 ns	$42 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5			245	485 ns	$218 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t _{PLH}		95	195 ns	$84 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			60	125 ns	$52 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
$CP_0, \overline{CP}_1 \rightarrow \overline{O}_{4-7}$ HIGH to LOW	5			245	485 ns	$218 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t _{PHL}		90	185 ns	$79 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			60	120 ns	$52 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5			190	380 ns	$163 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t _{PLH}		75	145 ns	$64 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			50	105 ns	$42 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
MR $\rightarrow O_1$ to O_7 HIGH to LOW	5			130	260 ns	$103 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t _{PHL}		55	105 ns	$44 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			40	75 ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
MR $\rightarrow O_0$ LOW to HIGH	5			130	260 ns	$103 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t _{PLH}		55	105 ns	$44 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			40	75 ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
MR $\rightarrow \overline{O}_{4-7}$ LOW to HIGH	5			110	220 ns	$83 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t _{PLH}		45	90 ns	$34 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			35	70 ns	$27 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5			60	120 ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10	t _{THL}		30	60 ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15			20	40 ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5			60	120 ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10	t _{TLH}		30	60 ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15			20	40 ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

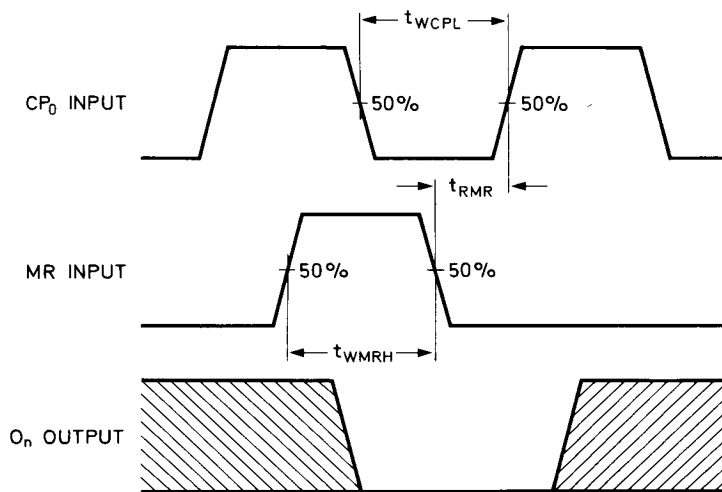
	V_{DD} V	symbol	min.	typ.	max.	
Hold times $CP_0 \rightarrow \overline{CP}_1$	5	t_{hold}	140	70	ns	see also waveforms Figs 4 and 5
	10		50	25	ns	
	15		30	15	ns	
$\overline{CP}_1 \rightarrow CP_0$	5	t_{hold}	170	85	ns	
	10		60	30	ns	
	15		40	20	ns	
Minimum clock pulse width	5	t_{WCP}	75	35	ns	
	10		30	15	ns	
	15		20	10	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	70	35	ns	
	10		30	15	ns	
	15		20	10	ns	
Recovery time for MR	5	t_{RMR}	30	10	ns	
	10		15	5	ns	
	15		10	5	ns	
Maximum clock pulse frequency	5	f_{max}	3	6	MHz	
	10		8	16	MHz	
	15		12	24	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$475 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10		f_o = output freq. (MHz)
	15		C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)



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Fig. 4 Waveforms showing hold times for CP_0 to \overline{CP}_1 and \overline{CP}_1 to CP_0 . Hold times are shown as positive values, but may be specified as negative values.



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Fig. 5 Waveforms showing recovery time for MR; minimum CP_0 and MR pulse widths.

Conditions: $\overline{CP}_1 = \text{LOW}$ while CP_0 is triggered on a LOW to HIGH transition.

t_{WCP} and t_{RMR} also apply when $CP_0 = \text{HIGH}$ and \overline{CP}_1 is triggered on a HIGH to LOW transition.

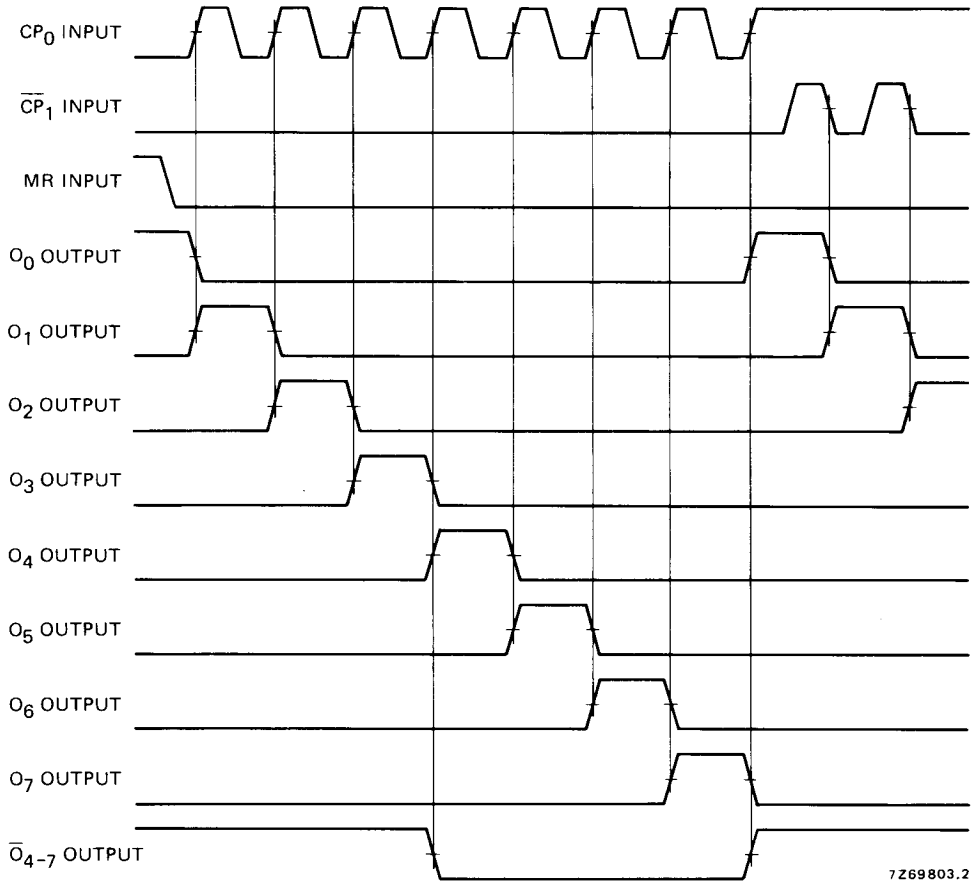


Fig. 6 Timing diagram.

APPLICATION INFORMATION

Some of the features of the HEF4022B are:

- High speed
- Spike-free decoded outputs
- Carry output for cascading

Figure 7 shows a technique for extending the number of decoded output states for the HEF4022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

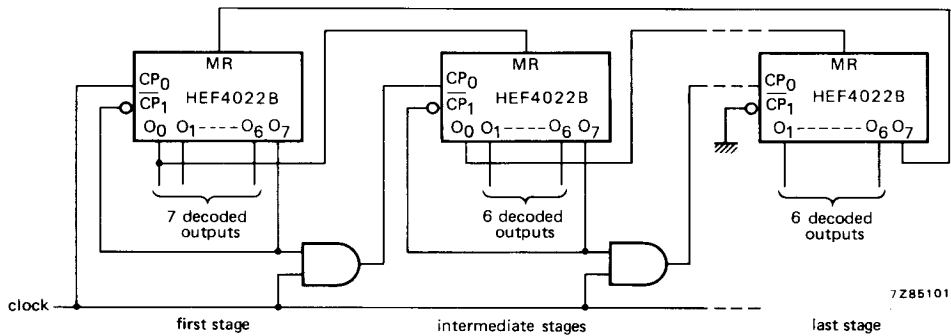


Fig. 7 Counter expansion.