LC7265, 7266

T-77-05-05

3025B

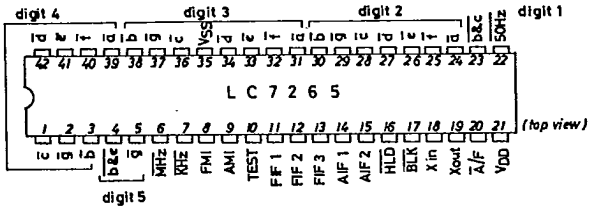
CMOS LSI

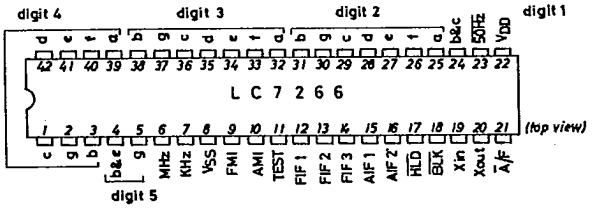
Receiving Frequency Display

Features

1. Displays received frequency of each band of FM, MW, LW
   LC7265 : LED static display
   LC7266 : FL static display
2. Counts local oscillation frequency and displays received frequency.
3. Number of display digits : FM-5 digits, MW-4 digits, LW-3 digits.
4. Covers intermediate frequencies shown below.
   FM : +10.700, +10.725, +10.750, +10.675 MHz
   −10.700, −10.725, −10.675, −10.650 MHz
   MW,LW : +450kHz : 10kHz step display
   +450kHz : 1kHz step display
   +455kHz : 1kHz step display
   +469kHz : 1kHz step display
5. Contains blanking circuit to turn off display
6. Contains hold circuit to hold display contents.
7. Uses crystal resonator having 7.2MHz reference frequency.
8. Uses LB3500 (÷8 prescaler) jointly at the time of FM reception.
9. Supply voltage V_{DD} : 4.5V to 10V

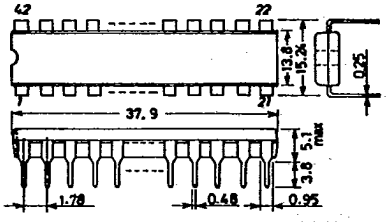
Pin Assignment





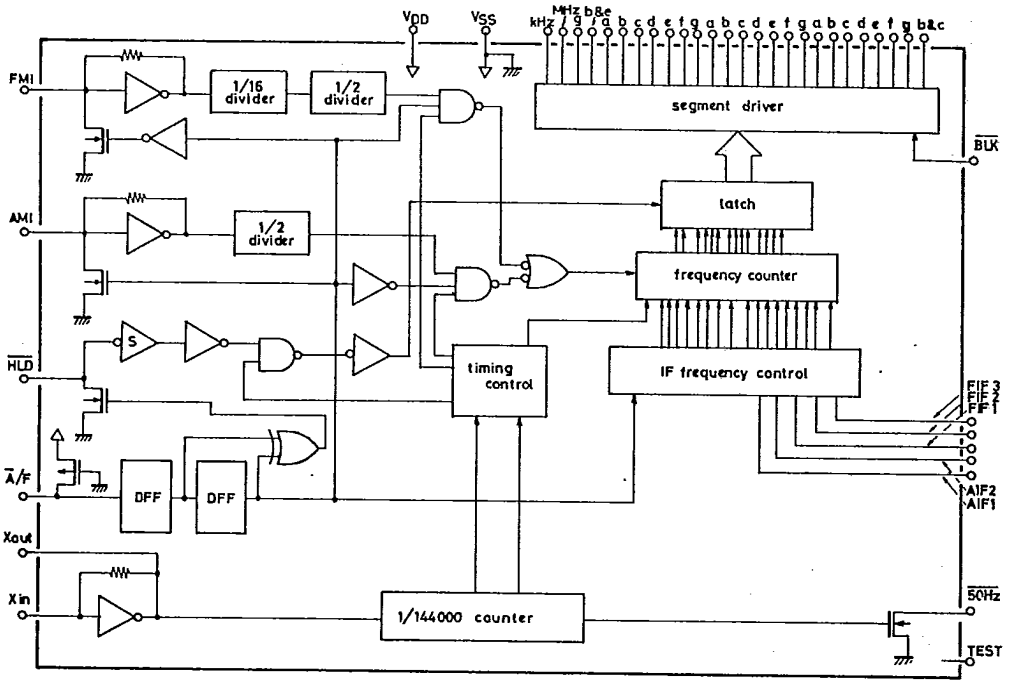
Case Outline 3025B-D42SIC

(unit : mm)



SANYO: DIP42S

Equivalent Circuit Block Diagram [LC7266]



Note) For the LC7265, attach – (bar) to output segment symbols.

1. Display

1-1 Display font

1 2 3 4 5 6 7 8 9 0

1-2 Lighting system

· Static lighting

1-3 Display range (High-order 1 digit : zero blanking)

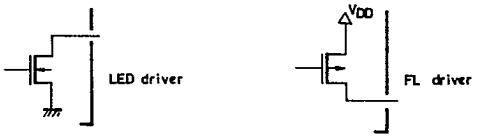
· FM : 00.00MHz to 199.95MHz 50kHz step

· MW,LW : 000kHz to 1999kHz 10kHz or 1kHz step

2. Pin Description

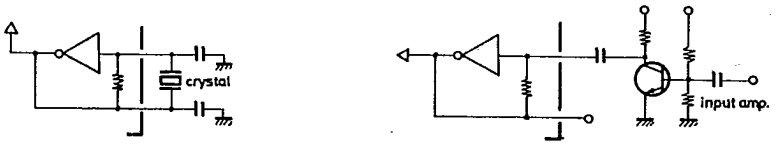
2-1 · $\overline{a}$ to $\overline{g}$,$\overline{b\&c}$,$\overline{b\&e}$,$\overline{MHz}$,$\overline{kHz}$: LED (LC7265)

· a to g,b&c,b&e,MHz,kHz : FL (LC7266)



2-2 · V_{DD},V_{SS} : Power supply pins

2-3 · X_{IN},X_{OUT} : Crystal resonator or input amp pin



2-4 · FIF(1),FIF(2),FIF(3) : FM IF select pins

FIF1	0	0	0	0	1	1	1	1
FIF2	0	0	1	1	0	0	1	1
FIF3	0	1	0	1	0	1	0	1
IF (MHz)	+10.700	+10.725	+10.675	+10.750	−10.700	−10.725	−10.675	−10.650

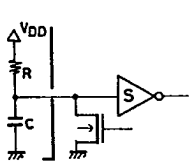
2-5 · AIF(1),AIF(2) : AM IF select pins

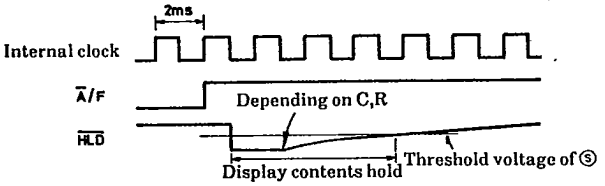
AIF1	0	0	1	1
AIF2	0	1	0	1
IF (kHz)	+450(2)	+450(1)	+455	+469

1 : High level (V_{DD})
0 : Low level (V_{SS})

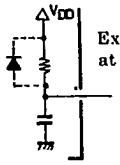
(Note) 450kHz(1) : 10kHz step display, others : 1kHz step display

2-6 · $\overline{HLD}$: Display contents hold pin
Normally, this pin is set at high level. To hold display contents, this pin is set at low level. Connecting time constant circuit to this pin makes it possible to hold display contents for a certain period of time at the time of FM/MW,LW band selection.





2-7 · $\overline{BLK}$: Display blanking pin

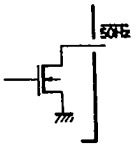


Example of blanking misdisplay at the time of application of power.

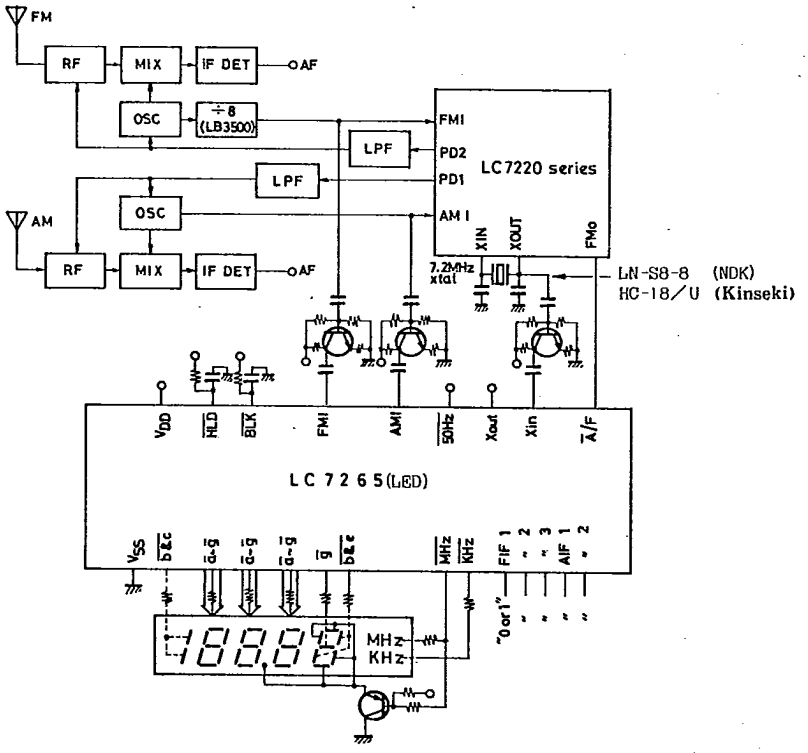
2-8 · FMI,AMI : Local oscillation signal input pins
FMI-----For FM : 0.7Vp-p input sensitivity
AMI-----For MW, LW : 1.0Vp-p input sensitivity (V_{DD}=8 to 10V, f_{IN}=0.5 to 0.9MHz)
0.5Vp-p input sensitivity (other than above)

2-9 · $\overline{A}$/F : FM/MW,LW select pin
FM-----Pin open or high level
MW,LW-----Low level

2-10 · $\overline{50Hz}$: 50Hz time base output pin



3. Sample Application Circuit (Using LC7265 jointly with LC7220 series)



4. Main Specifications

4-1 Main Specifications for LC7265

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

				unit
Maximum Supply Voltage	V_{DD} max		−0.3 to +11	V
Input Voltage	V_{IN}	All input pins	−0.3 to V_{DD}+0.3	V
Output Voltage	$V_{O(1)}$	X_{OUT}, $\overline{HLD}$, $\overline{50Hz}$, output : off	−0.3 to V_{DD}+0.3	V
Allowable Power Dissipation	Pdmax	Ta ≦ 65°C	550	mW
Allowable Power Dissipation of Segment Outputs	Pd(seg)	$\overline{MHz}$, $\overline{b\&c}$, $\overline{b\&e}$ V_{DD} = 4.5 to 6.5V, I_{OL} = 33mA	30	mW
Allowable Power Dissipation of Segment Outputs	Pd(seg)	Other outputs, V_{DD} = 4.5 to 6.5V, I_{OL} = 16.5mA	15	mW
Allowable Power Dissipation of Segment Outputs	Pd(seg)	$\overline{MHz}$, $\overline{b\&c}$, $\overline{b\&e}$, V_{DD} = 6.0 to 10V, I_{OL} = 36mA	25	mW
Allowable Power Dissipation of Segment Outputs	Pd(seg)	Other outputs, V_{DD} = 6.0 to 10V, I_{OL} = 18mA	12	mW
Operating Temperature	Topg		−30 to +65	°C
Storage Temperature	Tstg		−40 to +125	°C
Output Voltage	$V_{O(2)}$	Output pins other than $V_{O(1)}$	0 to 15	V

Allowable Operating Conditions at Ta = 25°C, V_{DD} = 4.5 to 10V, V_{SS} = 0			min	typ	max	unit
Supply Voltage	V_{DD}		4.5		10	V
Input "H"-Level Voltage	$V_{IH(1)}$	$\overline{A/F}$, $\overline{BLK}$	0.7V_{DD}		V_{DD}	V
Input "L"-Level Voltage	$V_{IL(1)}$	$\overline{A/F}$, $\overline{BLK}$	0		0.3V_{DD}	V
Input "H"-Level Voltage	$V_{IH(2)}$	FIF1,FIF2,FIF3,AIF1,AIF2	0.9V_{DD}		V_{DD}	V
Input "L"-Level Voltage	$V_{IL(2)}$	FIF1,FIF2,FIF3,AIF1,AIF2	0		0.1V_{DD}	V
Input Frequency	$f_{IN(1)}$	FMI,sine wave,capacitive coupling,$V_{IN(1)}$ = 0.7Vp-p	1		18	MHz
	$f_{IN(2)}$	AMI,sine wave,capacitive coupling,$V_{IN(2)}$ = 0.5Vp-p*	0.5		3	MHz
	$f_{IN(3)}$	X_{IN}	0.2		7.5	MHz
Input Amplitude	$V_{IN(1)}$	FMI,sine wave,capacitive coupling,$f_{IN(1)}$ = 1 to 18MHz	0.7		0.9V_{DD}	Vp-p
	$V_{IN(2)}$	AMI,sine wave,capacitive coupling,$f_{IN(2)}$ = 0.5 to 3MHz	0.5*		0.9V_{DD}	Vp-p
	$V_{IN(3)}$	X_{IN},sine wave,capacitive coupling,$f_{IN(3)}$ = 0.2 to 7.5MHz	1.0		0.9V_{DD}	Vp-p
Segment Current	Iseg(1)	$\overline{MHz}$,$\overline{b\&e}$,$\overline{b\&c}$	0		30	mA
	Iseg(2)	Other outputs	0		15	mA

*: For $f_{IN(2)}$ = 0.5MHz to 0.9MHz and V_{DD} = 8 to 10V, $V_{IN(2)}$min = 1.0Vp-p applies.

Electrical Characteristics at Ta = 25°C, V_{DD} = 4.5 to 10V, V_{SS} = 0V			min	typ	max	unit
Input "H"-Level Current	$I_{IH(1)}$	FIF1,FIF2,FIF3, AIF1,AIF2 $V_I = V_{DD}$	0		10	μA
Input "L"-Level Current	$I_{IL(1)}$	FIF1,FIF2,FIF3, AIF1,AIF2 $V_I = V_{SS}$	0		10	μA
Input "H"-Level Current	$I_{IH(2)}$	$\overline{BLK}$ $V_I = V_{DD}$	0		2	μA
Input "L"-Level Current	$I_{IL(2)}$	$\overline{BLK}$ $V_I = V_{SS}$	0		2	μA
Input "L"-Level Current	$I_{IL(3)}$	$\overline{A/F}$ $V_I = V_{SS}$	20		500	μA
Input Floating Voltage	$V_{IF(1)}$	$\overline{A/F}$ V_I = open	0.8V_{DD}		V_{DD}	V
Input/Output "H"-Level Leakage Current	$I_{OFF(1)}$	$\overline{HLD}$,output off,$V_I = V_{DD}$	0		2	μA
Output "L"-Level Voltage	$V_{OL(1)}$	$\overline{HLD}$,output on,I_O = 1mA	0		1	V
Input "H"-Level Threshold Voltage	V_{th}	$\overline{HLD}$	0.4V_{DD}	0.5V_{DD}	0.7V_{DD}	V
Output "L"-Level Voltage	$V_{OL(2)}$	$\overline{b\&e}$,$\overline{b\&c}$,$\overline{MHz}$ V_{DD} = 4.5 to 10V,I_{OL} = 30mA	0		0.7	V
Output "L"-Level Voltage	$V_{OL(3)}$	Segments other than above V_{DD} = 4.5 to 10V,I_{OL} = 15mA	0		0.7	V
Output "L"-Level Voltage	$V_{OL(4)}$	$\overline{50Hz}$,I_O = 0.2mA	0		1.0	V
Output Off Leakage Current	$I_{OFF(2)}$	All segments output pins, V_O = 13V,output off	0		10	μA
Current Dissipation	I_{DD}	FM mode,$\overline{A/F}$ = open or V_{DD} $f_{IN(1)}$ = 18MHz,0.7Vp-p or (AM mode,$\overline{A/F}$ = V_{SS}, $f_{IN(2)}$ = 3MHz,0.5Vp-p) $f_{IN(3)}$ = 7.2MHz,1Vp-p FIF1,FIF2,FIF3 = V_{DD} AIF1,AIF2 = V_{DD} $\overline{HLD}$,$\overline{BLK}$ = V_{DD} other pins open	0		18	mA

4-2 Main Specification for LC7266

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V				unit
Maximum Supply Voltage	V_{DD} max		−0.3 to +11	V
Input Voltage	V_{IN}		−0.3 to V_{DD}+0.3	V
Output Voltage	$V_{O(1)}$	X_{OUT}, $\overline{HLD}$, $\overline{50Hz}$, output off	−0.3 to V_{DD}+0.3	V
Output Voltage	$V_{O(2)}$	Output pins other than $V_{O(1)}$	V_{DD}−20 to V_{DD}+0.3	V
Allowable Power Dissipation	Pd max	Ta < 75°C	300	mW
Allowable Power Dissipation of Segment Output	Pd(seg)	MHz, $\lvert -I_{OH}\rvert$ < 18mA, Ta < 75°C	9	mW
Allowable Power Dissipation of Segment Output	Pd(seg)	b&c, b&e, $\lvert -I_{OH}\rvert$ < 6mA, Ta < 75°C	3	mW
Allowable Power Dissipation of Segment Output	Pd(seg)	Other outputs, $\lvert -I_{OH}\rvert$ < 3mA, Ta < 75°C	1.5	mW
Operating Temperature	Topg		−30 to +75	°C
Storage Temperature	Tstg		−40 to +125	°C

Allowable Operating Conditions at Ta = 25°C, V_{DD} = 4.5 to 10V, V_{SS} = 0V			min	typ	max	unit
Supply Voltage	V_{DD}		4.5		10	V
Input "H"-Level Voltage	$V_{IH(1)}$	$\overline{A/F}$, $\overline{BLK}$	0.7V_{DD}		V_{DD}	V
Input "L"-Level Voltage	$V_{IL(1)}$	$\overline{A/F}$, $\overline{BLK}$	0		0.3V_{DD}	V
Input "H"-Level Voltage	$V_{IH(2)}$	FIF1, FIF2, FIF3, AIF1, AIF2	0.9V_{DD}		V_{DD}	V
Input "L"-Level Voltage	$V_{IL(2)}$	FIF1, FIF2, FIF3, AIF1, AIF2	0		0.1V_{DD}	V
Input Frequency	$f_{IN(1)}$	FMI, sine wave, capacitive coupling, $V_{IN(1)}$ = 0.7Vp-p	1		18	MHz
	$f_{IN(2)}$	AMI, sine wave, capacitive coupling, $V_{IN(2)}$ = 0.5Vp-p	0.5		3	MHz
	$f_{IN(3)}$	X_{IN}	0.2		7.5	MHz
Input Amplitude	$V_{IN(1)}$	FMI, sine wave, capacitive coupling, $f_{IN(1)}$ = 1 to 18MHz	0.7		0.9V_{DD}	Vp-p
	$V_{IN(2)}$	AMI, sine wave, capacitive coupling, $f_{IN(2)}$ = 0.5 to 3MHz	0.5*		0.9V_{DD}	Vp-p
	$V_{IN(3)}$	X_{IN}, sine wave, capacitive coupling, $f_{IN(3)}$ = 0.2 to 7.5MHz	1.0		0.9V_{DD}	Vp-p
Segment Current	Iseg(1)	MHz	0		9	mA
	Iseg(2)	b&e, b&c	0		3	mA
	Iseg(3)	Other outputs	0		1.5	mA

* : For $f_{IN(2)}$ = 0.5MHz to 0.9MHz and V_{DD} = 8 to 10V, $V_{IN(2)}$min = 1.0Vp-p applies.

Electrical Characteristics at Ta = 25°C, V_{DD} = 4.5 to 10V, V_{SS} = 0V			min	typ	max	unit
Input "H"-Level Current	$I_{IH(1)}$	FIF1, FIF2, FIF3, AIF1, AIF2 ($V_I = V_{DD}$)	0		10	µA
Input "L"-Level Current	$I_{IL(1)}$	FIF1, FIF2, FIF3, AIF1, AIF2 ($V_I = V_{SS}$)	0		10	µA
Input "H"-Level Current	$I_{IH(2)}$	$\overline{BLK}$ $V_I = V_{DD}$	0		2	µA
Input "L"-Level Current	$I_{IL(2)}$	$\overline{BLK}$ $V_I = V_{SS}$	0		2	µA
Input "L"-Level Current	$I_{IL(3)}$	$\overline{A/F}$ $V_I = V_{SS}$	20		500	µA
Input Floating Voltage	$V_{IF(1)}$	$\overline{A/F}$ V_I = open	0.8V_{DD}		V_{DD}	V
Input/Output "H"-Level Leakage Current	$I_{OFF(1)}$	$\overline{HLD}$, output off, $V_I = V_{DD}$	0		2	µA
Output "L"-Level Voltage	$V_{OL(1)}$	$\overline{HLD}$, output on, I_O = 1mA	0		1	V
Input "H"-Level Threshold Voltage	$V_{th(1)}$	$\overline{HLD}$	0.4V_{DD}	0.5V_{DD}	0.7V_{DD}	V
Output "H"-Level Voltage	$V_{OH(1)}$	MHz I_{OH} = −3mA	V_{DD}−1			V
	$V_{OH(2)}$	b&e, b&c, I_{OH} = −1mA	V_{DD}−1			V
	$V_{OH(3)}$	Segments other than above, I_{OH} = −0.5mA	V_{DD}−1			V

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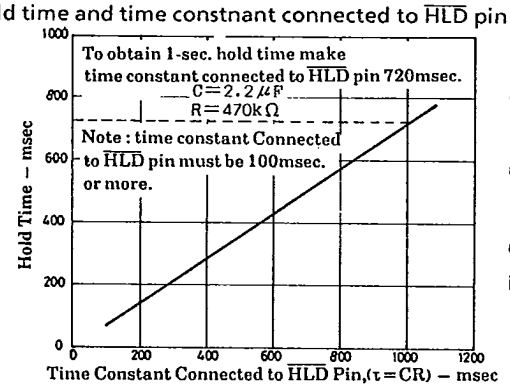
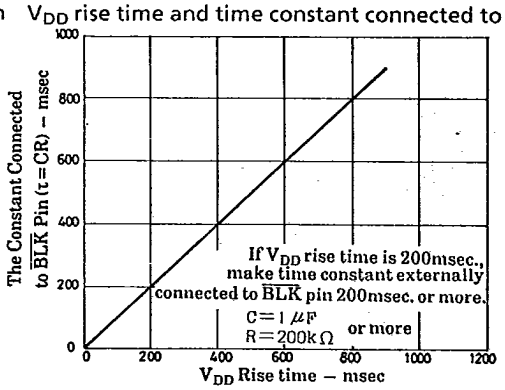
			min	typ	max	unit
Output "L"-Level Voltage	$V_{OL(2)}$	$\overline{50Hz}$ I_O=0.2mA	0		1.0	V
Output Off Leakage Current	$I_{OFF(2)}$	All segments output pins, $V_O=V_{DD}-18V$, output off	0		3	μA
Current Dissipation	I_{DD}	FM mode, $\overline{A}/F$=open or V_{DD} $f_{IN(1)}$=18MHz, 0.7Vp-p or AM mode, $\overline{A}/F=V_{SS}$ $f_{IN(2)}$=3MHz, 0.5Vp-p $f_{IN(3)}$=7.2MHz, 1Vp-p FIF1, FIF2, FIF3=V_{DD} AIF1, AIF2=V_{DD} $\overline{HLD}$, $\overline{BLK}$=V_{DD} other pins open	0		18	mA

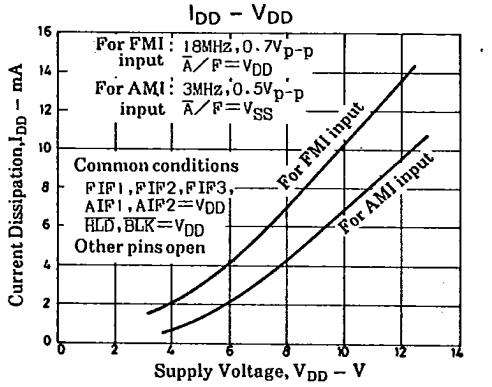
Hold time and time constnant connected to $\overline{HLD}$ pin



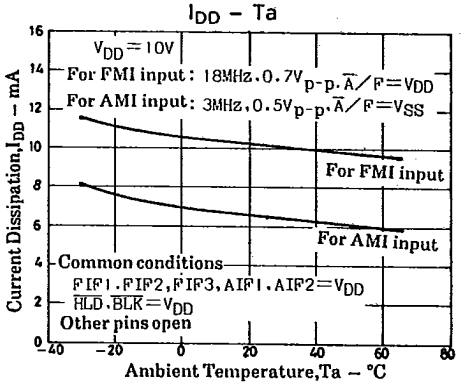
V_{DD} rise time and time constant connected to $\overline{BLK}$ pin



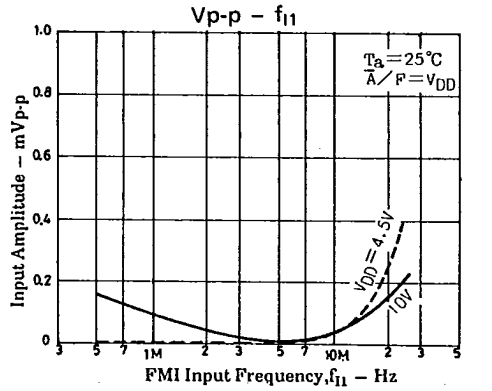
I_{DD} – V_{DD}



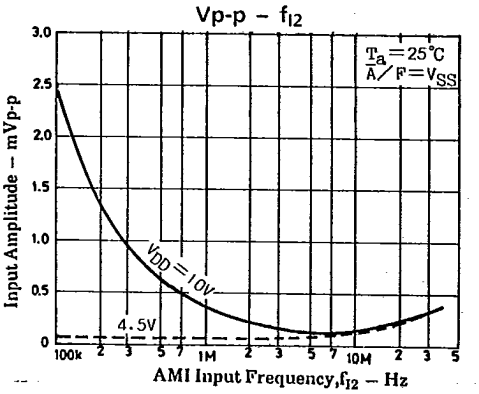
I_{DD} – Ta



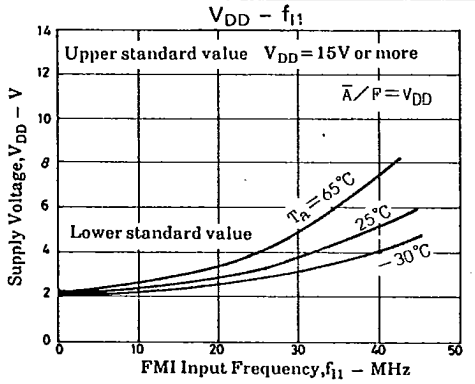
Vp-p – f_{I1}



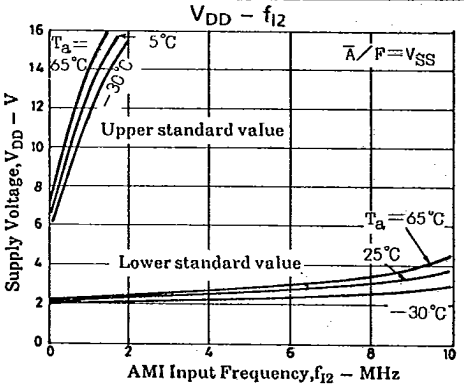
Vp-p – f_{I2}



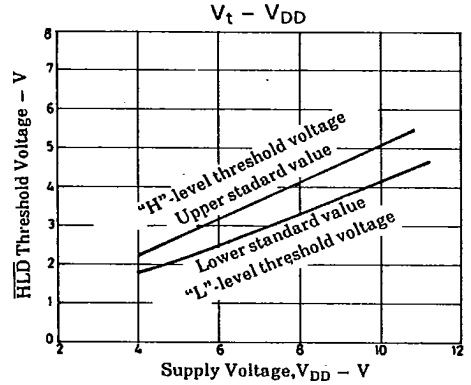
$V_{DD} - f_{I1}$



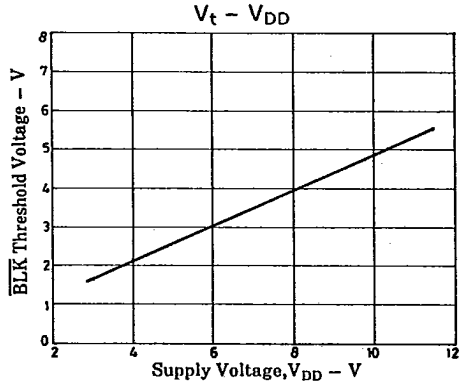
$V_{DD} - f_{I2}$



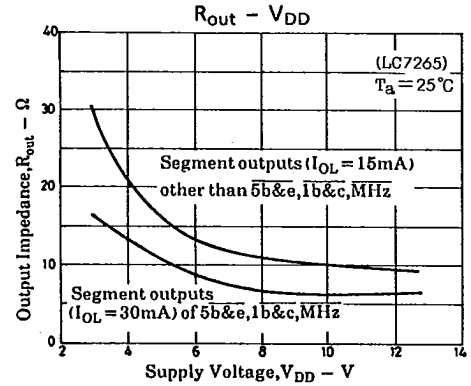
$V_t - V_{DD}$



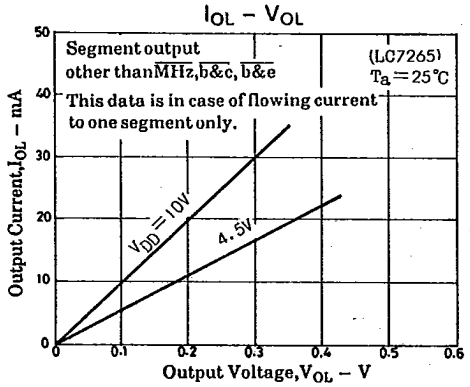
$V_t - V_{DD}$



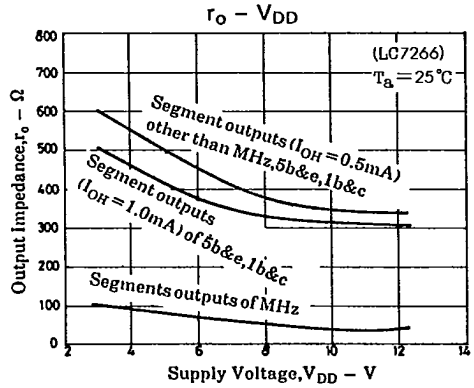
$R_{out} - V_{DD}$



$I_{OL} - V_{OL}$



$r_o - V_{DD}$



$I_{OH} - (V_{DD} - V_{OH})$