1.0 INTRODUCTION

The TSP53C30 is a programmed TSP50C41 that operates as a slave device to a microprocessor. The TSP53C30 includes a 10 pole Linear Predictive Filter (the synthesizer) an 8K ROM and an 8-bit microprocessor. The speech synthesizer operates on Linear Predictive Code (LPC) or Pulse Code Modulated (PCM) speech data. Detailed information on the TSP50C41 is contained in the "TSP50C4X Family Speech Synthesizers, Design Manual".

Unless otherwise noted data and commands are specified in hexadecimal format. Quantities are given as decimal numbers.

1.1 INTRODUCTION TO LPC

The LPC-10 system uses a mathematical model of the human vocal tract to enable efficient digital storage and re-creation of realistic speech. To understand LPC it is essential to understand how the vocal tract works. This introduction therefore, begins with a short description of the vocal tract. The LPC model and data compression techniques are then addressed. A short discussion of the techniques and pitfalls of collecting, analyzing, and editing speech for LPC synthesis is included in Appendix I. For more information contact your TI Field Sales Representative or Regional Technology Center.

1.1.1 THE VOCAL TRACT

Speech is the result of the interaction between three elements in the vocal tract, air from the lungs, a restriction which converts the air flow to sound and the vocal cavities which are positioned to resonate properly.

The air from the lungs is expelled through the vocal tract when the muscles of the chest and diaphragm are compressed. Pressure is used as a volume control, higher pressure for louder speech.

As air flows through the vocal tract it makes very little sound if there is no restriction. The vocal cords are one type of restriction. They can be tightened across the vocal tract to stop the flow of air. Pressure builds up behind them and forces them open. This happens over and over, generating a series of pulses. The tension on the vocal cords can be varied, to change the frequency of the pulses. Many speech sounds are produced by this type of restriction, for example, the "A" sound. This is called "voiced" speech.

A different type of restriction takes place in the mouth and causes a hissing sound called white noise. The "S" sound is a good example. This occurs when the tongue and some part of the mouth are in close contact or when the lips are pursed. This restriction causes high flow velocities which cause turbulence that produces white noise. This is called "unvoiced" speech.

The pulses from the vocal cords and the noise from the turbulence have fairly broad, flat spectral characteristics. In other words, they are really noise, not speech. The shape of the oral cavity changes noise into recognizable speech. The position of the tongue, the lips and the jaws change the resonance of the vocal tract, shaping the raw noise of restricted airflow into understandable sounds.

1.1.2 THE LPC MODEL

The LPC model incorporates elements analogous to each of the elements of the vocal tract described above. It has an excitation function generator that models both types of restriction, a gain multiplication stage to model the possible levels of pressure from the lungs, and a digital filter to model the resonance in the oral and nasal cavities.

Figure 1.4 shows the LPC model in schematic form. The excitation function generator accepts coded pitch information as an input and can generate a series of pulses similar to vocal cord pulses. It can also generate white noise. The waveform is then multiplied by an energy factor that corresponds to the pressure from the lungs. Finally, the signal is passed through a digital filter that models the shape of the oral cavity. In the TSP53C30, this filter has ten poles, so the synthesis is referred to as LPC-10.

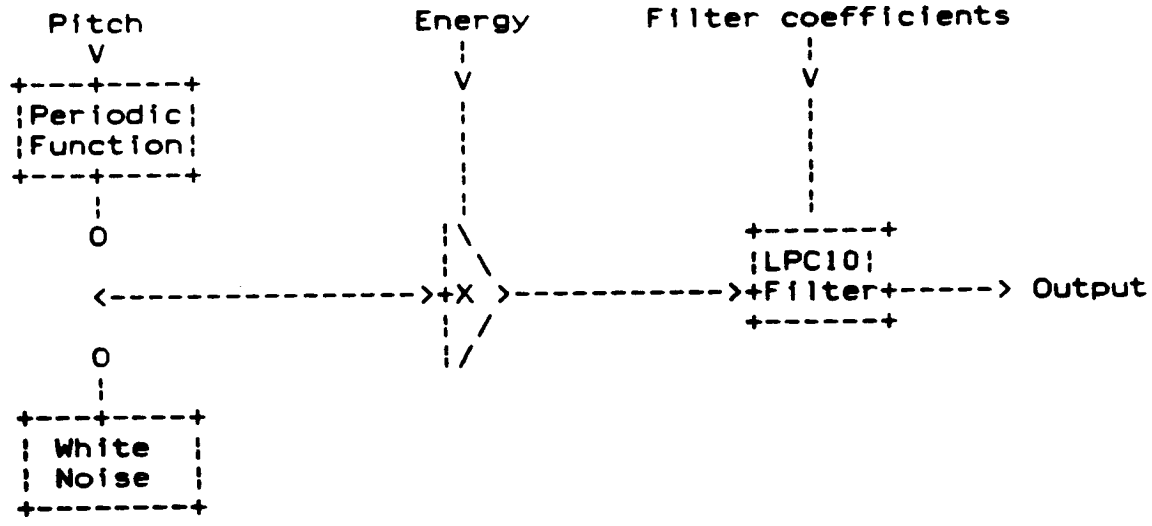


Figure 1-1
LPC-10 VOCAL TRACT MODEL

1.1.3 LPC DATA COMPRESSION

The data compression for LPC-10 takes advantage of other characteristics of speech. Speech changes fairly slowly, and the oral and nasal cavities tend to fall into certain areas of resonance more than others. The speech is analyzed in frames that are generally 20 milliseconds long. The inputs to the model are calculated as an average for the entire frame. The synthesizer smooths or interpolates the data during the frame, so there isn't an abrupt transition at the end of each frame. Often speech changes even more slowly than the frame. TI's LPC model allows for a repeat frame, where the only values changed are the pitch and the energy. The filter coefficients are kept constant from the previous frame. To take advantage of the recurrent nature of resonance in the oral cavity, all the coefficients are encoded, with values from three to six bits for each coefficient. The coding table is designed so that more coverage is given to the coefficient values that occur frequently.

1.2 FEATURES

The TSP53C30 is compatible with TSP5220 speech data. Existing data may require bit reversing within each byte but this task is easily performed with a high level language such as C or PASCAL. Appendix F is a TURBO PASCAL listing for a program that performs the bit reversing operation.

The TSP53C30 can be put directly on the data bus for many microprocessors. Speech data is stored and controlled by the host processor and passed to the TSP53C30 via the data bus. Appendix E is an example of the TSP53C30 interfaced to a TMS7000 microprocessor.

The TSP53C30 will accept data in the new Texas Instruments D6 format. Speech data in this format has a slightly higher bit rate and finer resolution for pitch control than the TSP5220 speech data.

PCM data is accepted by the TSP53C30. This data format results in a very high data rate but provides the user with the capability of producing sound effects that are not possible with LPC encoded speech data.

The TSP53C30 accepts Pre-decoded speech data. This is speech data that has not been encoded and packed, such as the TSP5220 and D6 data. Or it is TSP5220 or D6 data that has been unpacked and decoded external to the TSP53C30. This mode of operation gives the user very fine control over the speech parameters.

Speech data can also be stored in a Texas Instruments VROM (Vocabulary ROM). The VROM will interface directly to the TSP53C30 so that the host microprocessor does not have to store and handle the speech data.

1.3 APPLICATIONS

The TSP53C30 can be interfaced to a microcontroller or a microprocessor bus. TSP53C30 clock and analog output signals are not shown in the block diagrams in this section. A detailed interconnect for an interface to a TMS7000 microprocessor is shown in Appendix E.

Since the TSP53C30 will power down after completing a word or phrase it is ideally suited for systems that are battery powered. In the power down mode the TSP53C30 only requires a maximum of 50 micro-amperes at 5 volts.

Note that for the applications that are shown in this manual the ENA1~ and ENA2~ pins are connected together. This is the configuration used when the TSP53C30 is interfaced to an eight bit data bus. If a four bit data bus is used two Read or two Write cycles are required to transfer each byte of data. See Table 1-1 for a description of the functions performed by each enable pin.

Applications for the TSP53C30 include:

- Computer speech modules
- Vending machines
- Hand-held talking check lists
- Security systems with battery backup
- Automobile warning systems
- Aircraft warning systems
- Talking calculators
- Educational games

1.3.1 MICROCONTROLLER INTERFACE

The TSP53C30 can be interfaced to a host processor such as a microcontroller (uC). This configuration will produce a minimum parts count speech system. Systems that have a small amount of speech would put the data in the uC's internal memory.

If the speech requirements are too great for the uC's internal memory capacity the data can be stored in a TSP60C20 Vocabulary ROM (VROM). The data can also be put into an EPROM that is addressed by the uC.

A uC/TSP53C30 configuration is shown in figure 1-2.

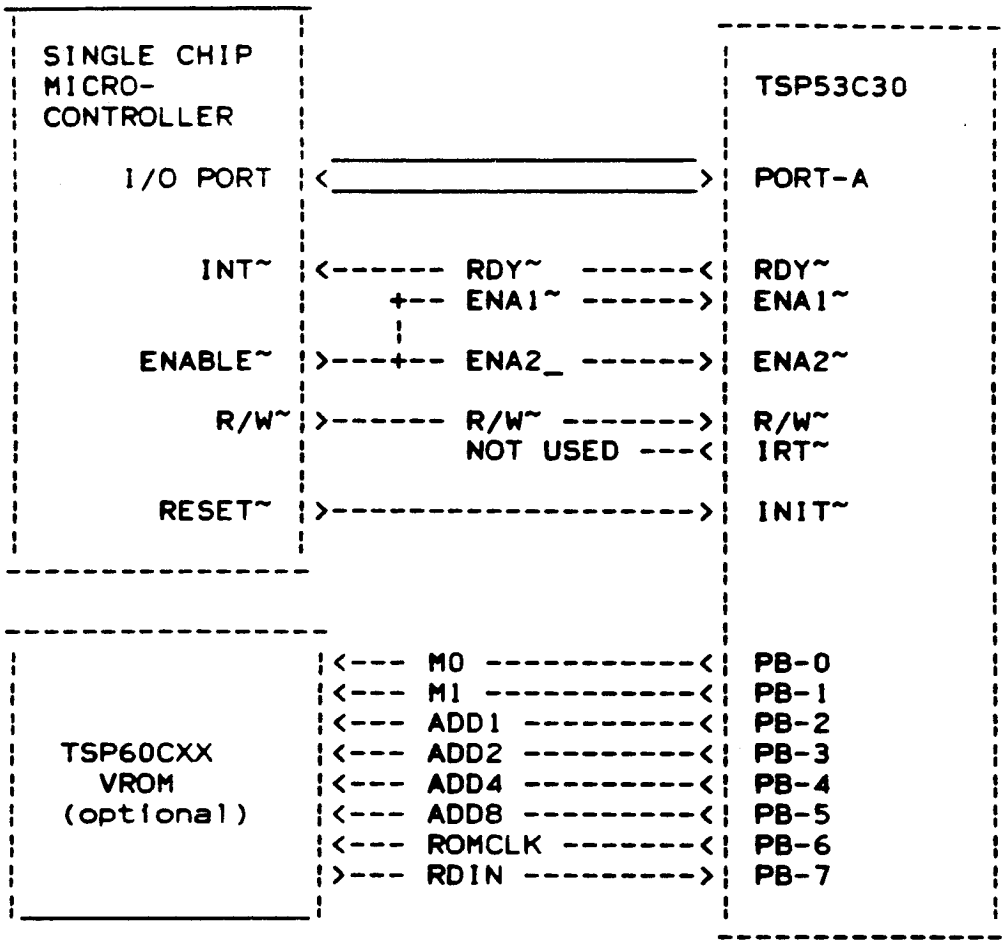


Figure 1-2
TSP53C30 WITH A MICROCONTROLLER INTERFACE AND OPTIONAL VROM

Application block diagram of the TSP53C30 used with a single chip microcontroller. Speech data in this example is stored in both the microcontroller memory and in the TSP60C20 VROM. For a very small system, all the speech data could be stored inside the microcontroller thus eliminating the TSP60C20 VROM.

1.3.2 MICROPROCESSOR INTERFACE

The TSP53C30 is optimized for use with a microprocessor (uP) based system. Figure 1-3 is a block diagram of a system that includes a TMS7000 uP. The TSP53C30 requires an initialization signal at the start of each speech phrase, therefore, one of the TMS7000's memory addresses is dedicated to initializing the synthesizer.

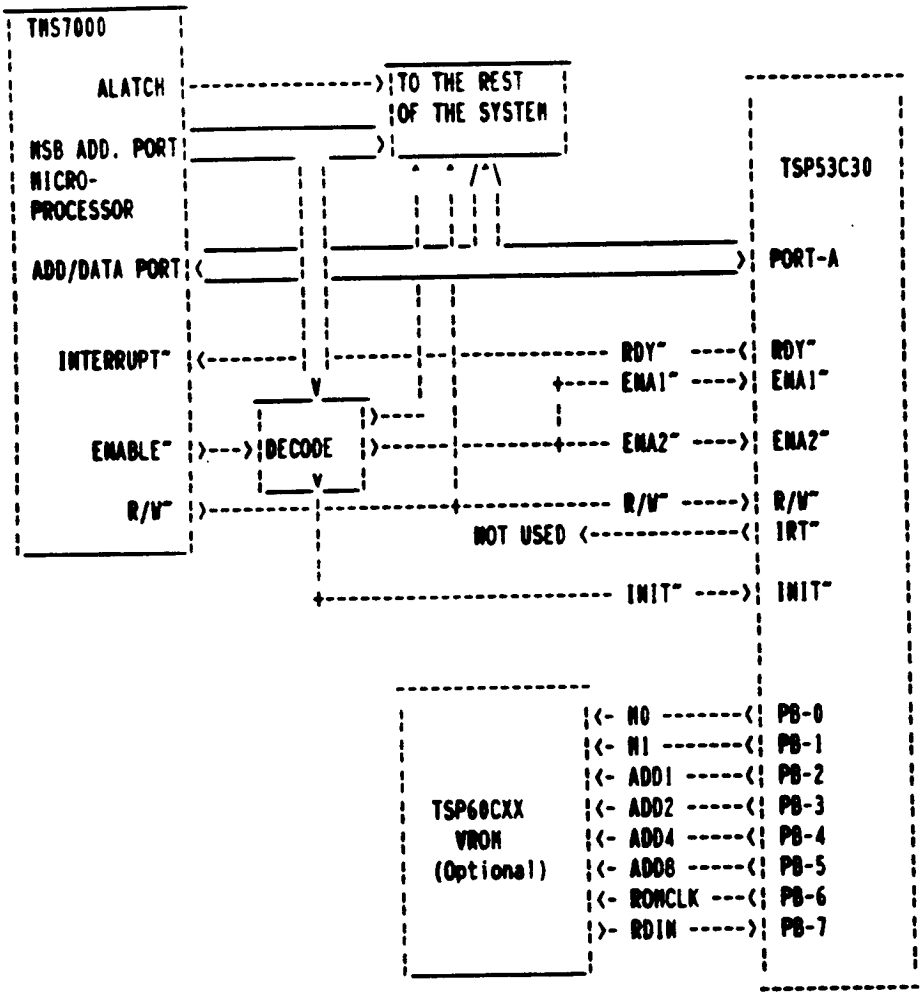


Figure 1-3
TSP53C30 WITH A MICROPROCESSOR INTERFACE AND OPTIONAL VROM

Application block diagram of the TSP53C30 used with a general purpose microprocessor and a TSP60CXX VROM. Speech data is typically stored only in the uP system memory, but the TSP60C20 VROM gives added storage capacity and system flexibility.

1.4 PIN ASSIGNMENT AND DESCRIPTION

N2 PACKAGE - TOP VIEW

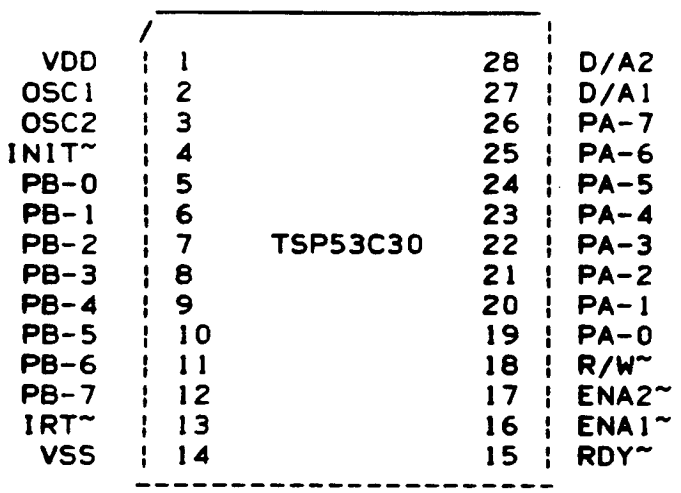


Figure 1-4
PIN ASSIGNMENTS

PIN NO.	NAME	I/O	DESCRIPTION
1	VDD	I	4.0 - 6.3 VDC.
2	OSC1	I	OSCILLATOR. 3.07 MHZ or 3.84 MHZ ceramic resonator or crystal. Alternately a CMOS clock can be applied to pin 2. If pin 4 is low the internal clock will stop.
3	OSC2	I	
4	INIT~	I	INITIALIZE BAR. Active low input that initializes the TSP53C30.
5	M0	O	MODE BIT 0. \
6	M1	O	MODE BIT 1. |
7	ADD1	O	ADDRESS 1. |
8	ADD2	O	ADDRESS 2. |-- Interface to a TSP60C20 VROM.
9	ADD4	O	ADDRESS 4. | Pin 12 will only be an input pin when the TSP53C30 has been commanded to operate in the VROM mode. Otherwise it will be an output pin and will not require termination.
10	ADD8	O	ADDRESS 8. |
11	ROMCLK	O	ROM CLOCK. |
12	RDIN	I	READ IN. /

Table 1-1
PIN FUNCTION DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
13	IRT~	O	INTERRUPT REQUEST BAR. Active low output that indicates that a status or request word is available on Port-A. Normally not used since READY BAR can be used as an interrupt request.
14	VSS		GROUND.
15	RDY~	O	READY BAR. Open Drain, active low output that indicates a status or request word is available on Port-A. READY BAR will remain low until the host processor writes the requested data. Then RDY~ is set high when when ENA2~ is pulled low.
16	ENA1~	I	ENABLE-1 BAR AND ENABLE-2 BAR. Active low inputs that enable the reading or writing or Port-A data. Read mode (R/W~ high) ENA1~: Most significant nibble of the Port-A latch is put on the bus PA4-PA7 while ENA1~ is low. When ENA1~ goes low, IRT~ goes high. ENA2~: Least significant nibble of the Port-A latch is put on the bus PA0-PA3 while ENA2~ is low. Write mode (R/W~ low) ENA1~: Most significant nibble on the data bus PA4-PA7 is strobed into the Port-A latch when ENA1~ goes from low to high. ENA2~: Least significant nibble on the data bus PA0-PA3 is strobed into the Port-A latch when ENA2~ goes from low to high.
17	ENA2~	I	
18	R/W~	I	READ/WRITE BAR. READ from the TSP53C30 when high and WRITE to the TSP53C30 when low.
19	PA-0	I/O	PORT A. Bidirectional port used by the TSP53C30 for issuing data/address requests and status information and recieving speech data and data addresses from the host processor.
20	PA-1	I/O	
21	PA-2	I/O	
22	PA-3	I/O	
23	PA-4	I/O	
24	PA-5	I/O	
25	PA-6	I/O	
26	PA-7	I/O	
27	D/A1	O	DIGITAL/ANALOG. Pulse width modulated speech output.
28	D/A2	O	

Table 1-1 (continued)
PIN FUNCTION DESCRIPTION

2.0 ARCHITECTURE

Since the TSP53C30 is a programmed version of a TSP50C41 the hardware architecture is described in the TSP50C4X Design Manual. An overview of the software architecture is described by the block diagram in figure 2-1. The diagram does not show the speech data unpacking and decoding details. Nor does it show the interpolation, pitch/noise generator controls or the initialization for frames one and two.

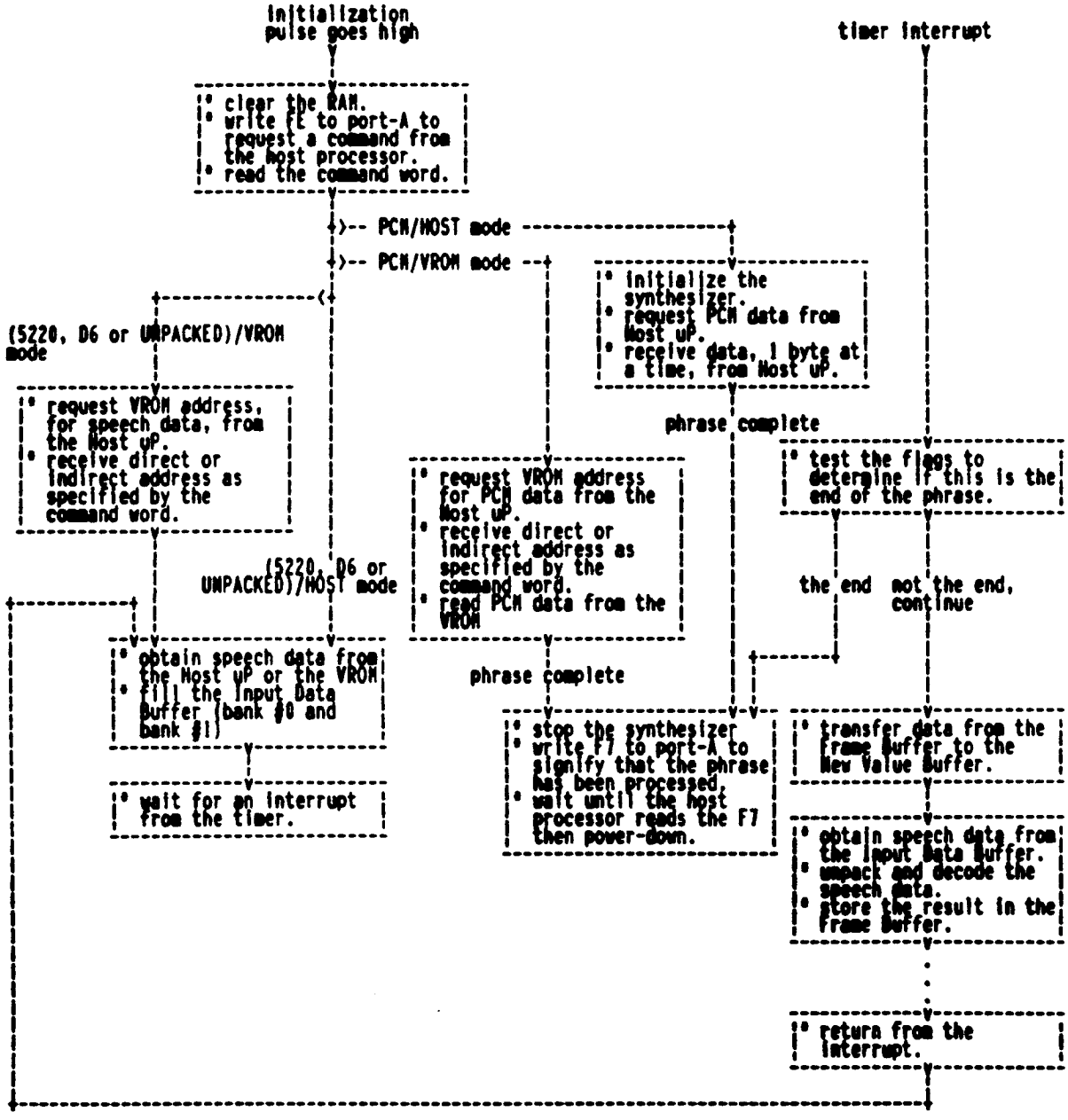


Figure 2-1
TSP53C30 software block diagram

2.1 SPEECH DATA FORMATS

The TSP53C30 can accept speech data in PCM, 5220, D6 and UNPACKED formats. PCM, 5220 and D6 speech data can be generated by the SDS-5000 Speech Development System. The data can also be developed by Texas Instruments. The procedure is described in Appendix A.

UNPACKED data is 5220 or D6 speech data that has been unpacked, decoded and reformatted. These three data formats, UNPACKED, 5220 and D6 provide the parameters for the TSP53C30's Linear Predictive Filter (the synthesizer). The PCM data is not modified by the filter but is passed through the synthesizer to the Digital-to-Analog Converter.

2.1.1 5220 SPEECH DATA

This is the same data that is used by the TSP5220 speech synthesizer, with the exception that the data has not been bit reversed. Appendix B describes the data format and the 5220 decoding table.

2.1.2 D6 SPEECH DATA

This speech data has a higher data rate than the 5220 data. This has been accomplished by adding an additional bit to data fields for the pitch parameter and the K1 through K4 reflection coefficient parameters. Appendix C describes the data format and the D6 decoding table.

2.1.3 UNPACKED SPEECH DATA

This is 5220 or D6 speech data that has been unpacked and decoded. The data rate for this format is about ten times higher than for the packed and coded 5220 or D6 formats. This format is used when it is necessary to change the speech frame period on a frame-to-frame basis or if the sound to be generated requires the highest possible resolution for the Energy, Pitch and Reflection Coefficient parameters (K1 through K10). The format for UNPACKED data is in Appendix D.

2.1.4 PCM SPEECH DATA

This is an eight bit two's complement data format. This data is generated by sampling a speech signal at 8k or 10K samples per second. The data rate for this format is about 100 times higher than for the packed and coded 5220 or D6 formats. This format is used when the highest quality speech sound is required or a non-vocal sound such as a tone must be produced.

2.2 OPERATING MODES

The TSP53C30 has twelve operating modes. They are defined the the data format, the memory used to store the data (Host microprocessor memory or VROM) and whether the data in the VROM will be located via a direct or indirect address.

In all modes of operation the speech data is stored external to the TSP53C30.

2.2.1 HOST MODE

PCM, 5220, D6 or UNPACKED Speech data is sent to the TSP53C30 by the Host microprocessor via Port-A. See figure 3-1 for the read-status/write-data sequence and figures 4-4 and 4-5 for the timing requirements.

2.2.2 VROM MODE, DIRECT ADDRESSING

PCM, 5220, D6 or UNPACKED Speech data is stored in the VROM. The speech data's address is sent to the TSP53C30 via Port-A. See figure 3-1 for the read-status/write-address data sequence and figures 4-4 and 4-5 for the timing requirements.

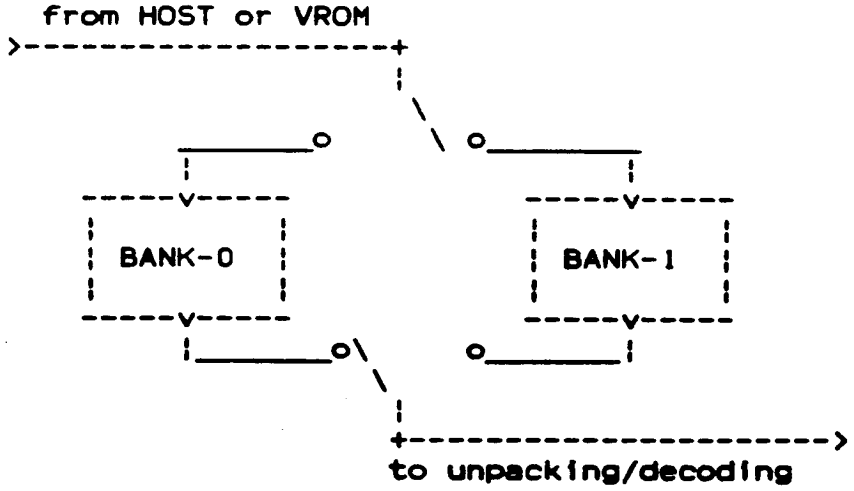
2.2.3 VROM MODE, INDIRECT ADDRESSING

PCM, 5220, D6 or UNPACKED Speech data is stored in the VROM. The Host microprocessor sends an indirect address to the TSP53C30 via Port-A. The TSP53C30 uses this address as a memory location where it will find the speech data's address. See figure 3-1 for the read-status/write-address data sequence and figures 4-4 and 4-5 for the timing requirements.

2.3 INPUT DATA BUFFER

Speech data is buffered in the TSP53C30 in all modes except PCM/HOST and PCM/VROM. In the PCM modes the data from the host processor or VROM is sent directly to the synthesizer. Because of the high PCM data rate there is not enough time to read the incoming data, store it in a buffer, read it from the buffer and send it to the synthesizer.

Data written to the TSP53C30 in non-PCM modes are internally buffered in RAM. There are two banks to the buffer, bank-0 and bank-1, schematically the buffer operation is:



The two banks are filled with data before unpacking and decoding is started. When a bank has been emptied the unpacking/decoding routines will switch to the other bank. If it is not full an "EF" status will be sent to the Host processor to indicate an abnormal stop. The TSP53C30 will then power down. If the other bank is full the unpacking/decoding will continue and the empty bank will be filled by the Host processor.

In the 5220/VROM and D6/VROM modes the buffer lengths are preset to 12 bytes. The length for the UNPACKED/VROM mode is preset to 21 bytes. For the 5220, D6 or UNPACKED/HOST modes the buffer length for each bank is determined by the operating command.

The 5220/HOST and D6/HOST modes use the two most significant bits in the command word to specify the buffer length as follows:

bit 7	bit 6	buffer length
0	0	8 bytes
0	1	16 bytes
1	0	24 bytes
1	1	32 bytes

A large buffer will minimize the number of times that the TSP53C30 has to be serviced. However, since the TSP53C30 will not use the data in a buffer bank unless the buffer is full it will be necessary, at the end of a word or phrase, to pad the buffer with extraneous data. A 32 byte buffer could require up to 31 bytes of extra data to fill the bank so that it will be available for use. A small buffer will minimize this problem but will require service more often than a larger buffer.

The UNPACKED/HOST mode requires a minumum of 15 bytes of data, as defined in Appendix D, to specify a speech frame. A frame can also have up to 6 additional bytes for the fractional parts of the K1 through K6 reflection coefficients. The three most significant bits in the command word specify the number of reflection coefficients, taken in sequence from K1 through K6;

bit 7	bit 6	bit 5	fractional reflection coefficients
0	0	0	none
0	0	1	K1
0	1	0	K1, K2
0	1	1	K1, K2, K3
0	0	0	K1, K2, K3, K4
1	0	1	K1, K2, K3, K4, K5
1	1	0	K1, 2K, K3, K4, K5, K6

2.4 SPEECH SPEED CONTROL

Bit 5 of the operation command word is used to set the speed of the speech in the 5220/HOST, 5220/VROM, D6/HOST and D6/VROM modes. If the bit is a 0 the speech will be spoken at its normal rate. If the bit is a 1 the speech rate will increase by 47%.

3.0 OPERATING PROCEDURES

All modes of operation are initiated by the signal on the INIT~ pin transitioning from low to high. If the pin is allowed to go low again the TSP53C30 will stop operation and go into the power down mode.

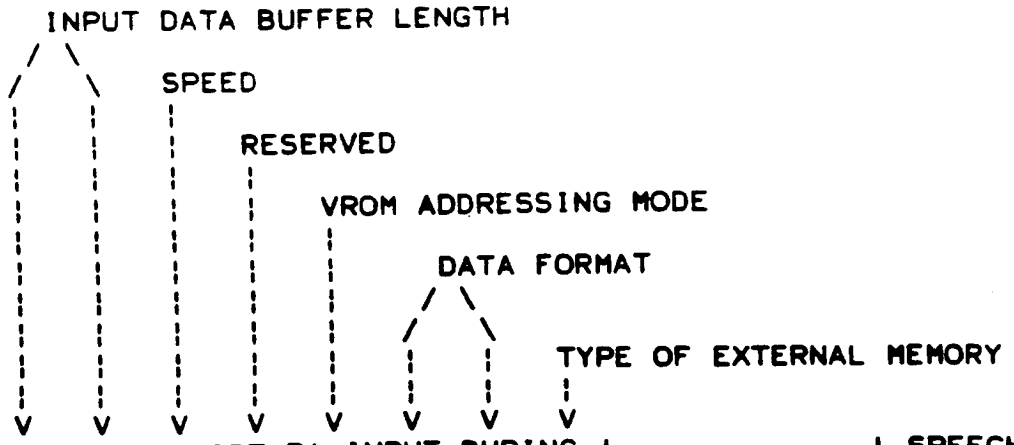
Table 3-1 lists the commands that are sent to the TSP53C30 to put the synthesizer in it's various modes. Table 3-2 lists the status words that are received from the TSP53C30.

Data/command/address/status transfers to and from the TSP53C30 are all byte-wide words.

The TSP53C30 is initialized at the beginning of each word (or phrase) by pulsing the INIT~ pin low then high. The TSP53C30 will stay in the power down mode as long as the INIT~ pin remains low. After the INIT~ pin goes high the normal routine will be:

TSP53C30	HOST PROCESSOR
a. Put an "FE" in the Port-A latch. Pull the RDY~ line low.	
	b. Detect the RDY~ line going low. Decode the request code. Write the Operating mode Command to Port-A. When the ENA2~ line is pulled low the RDY~ line will go high.
c. Put an "FD" (request speech data address) or "FB" (request speech data) in the Port-A latch. Pull the RDY~ line low.	
	d. Detect the RDY~ line going low. Decode the request code. Write the speech data or address to Port-A. When the ENA2~ line is pulled low the RDY~ line will go high.
e. Repeat (c.) and (d.) until the TSP53C30 detects a stop code at the end of a word or phrase.	
f. Stop code detected. Put an "F7" in the Port-A latch. Pull the RDY~ line low.	
	g. Detect the RDY~ line going low. Decode the status code.
h. Power down when the Host processor reads the "F7" status code.	

Figure 3-1 shows the Read/Write cycle for putting Commands, Speech Data and Speech Data Addressing into the TSP53C30. The timing requirements for the Read and Write cycles are given in Figures 4-4 and 4-5.



PORT P1 INPUT DURING INITIALIZATION									
7	6	5	4	3	2	1	0	DATA FORMAT	SPEECH DATA SOURCE
0	0	0	0	0	0	0	0	PCM	HOST uP
n1	n0	s	0	0	1	1	0	5220	HOST uP
n1	n0	s	0	0	1	0	0	D6	HOST uP
p2	p1	p0	0	0	0	1	0	UNPACKED	HOST uP
0	0	0	0	i	0	0	1	PCM	VROM
0	0	s	0	i	1	1	1	5220	VROM
0	0	s	0	i	1	0	1	D6	VROM
0	0	0	0	i	0	1	1	UNPACKED	VROM

NOTE:

n1, n0 = The Length of each bank in the Input Data Buffer.
00 --> 8 BYTES
01 --> 16 BYTES
10 --> 24 BYTES
11 --> 32 BYTES

p2, p1, p0 = The number of unpacked fractional K parameters that that will be passed to the TSP53C30 by the host processor.

s = The frame rate for 5220 and D6 encoded speech data.
0 --> 50 frames per second (10 KHz sampling rate)
1 --> 73.5 frames per second (10 KHz sampling rate)

i = VROM speech data addressing mode
0 --> direct addressing
1 --> indirect addressing

Table 3-1
TSP53C30 operating modes and command words.

STATUS WORD								HEX	STATUS DESCRIPTION
7	6	5	4	3	2	1	0		
1	1	1	1	1	1	1	0	FE	WAITING FOR THE OPERATING MODE COMMAND.
1	1	1	1	1	1	0	1	FD	WAITING FOR THE SPEECH DATA ADDRESS.
1	1	1	1	1	0	1	1	FB	WAITING FOR SPEECH DATA.
1	1	1	1	0	1	1	1	F7	END OF SPEECH. STOP CODE DETECTED.
1	1	1	0	1	1	1	1	EF	ABNORMAL SPEECH STOP. OUT OF DATA.

Table 3-2
TSP53C30 Status words

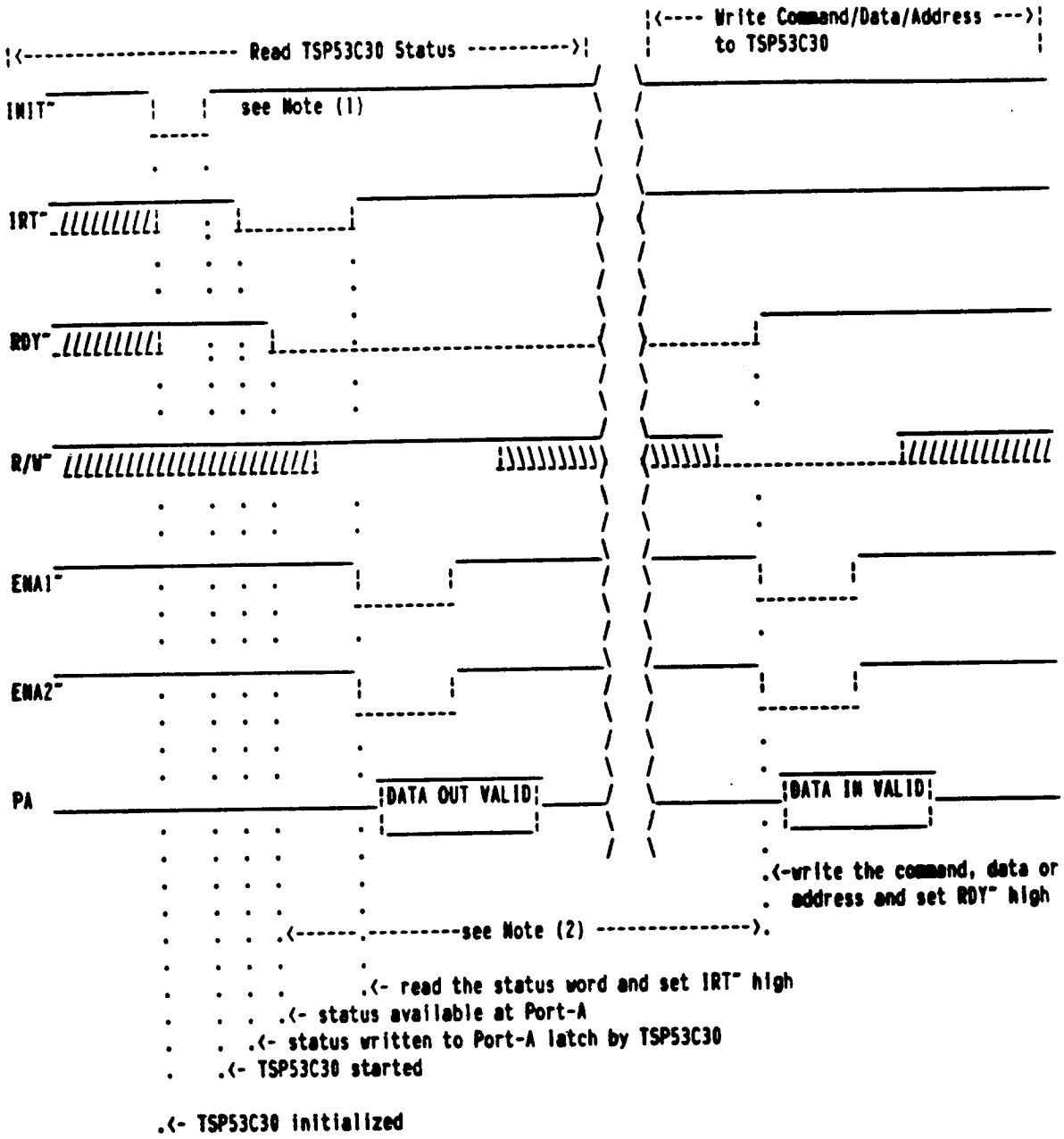
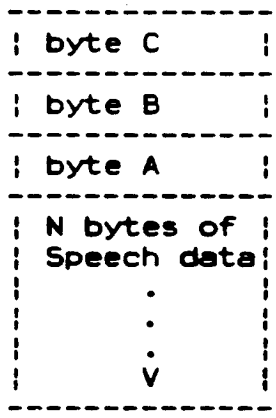


Figure 3-1
Read/Write sequence for Commands, Data and Addresses

Note: (1) The INIT~ pin only changes from low to high at the start of a Read/Write sequence for a new word or phrase.
(2) The TSP53C30 pulls RDY~ low by writing to a transparent latch. It will hold RDY~ low for a maximum of 32 clock periods (8.33 microseconds for a 3.84 MhZ clock). Therefore, wait 32 clock periods before writing the Command/Data/Address to the TSP53C30.

3.1 PCM/HOST MODE PROCEDURE

The speech data is sent to the TSP53C30 as two's complement data. The data is preceded by three bytes that specify the number of data bytes. The format for these three bytes is:



N is equal to:

$$(65{,}281 \times C) + (256 \times B) + A + 3 = N$$

Where;

C --- The first byte in the data file
B --- The second byte in the data file
A --- The third byte in the data file
N --- The number of PCM data bytes that are being defined by C, B, and A.

In the PCM mode the synthesizer must receive one byte, of speech data, every twelve TSP50C41 instruction cycles. This is every 100 microseconds for a clock frequency of 3.84 MhZ. Therefore, the data must be written to the TSP50C30 at a rate of one byte every twelve instruction cycles. The sequence of of operation is:

a. Cycle the INIT~ pin so that it makes a low-to-high transition.
b. TSP53C30 will pull RDY~ low.
c. Read the data on Port-A. It will be an "FE" (request operating mode command).
d. Write the command "00" (PCM/HOST mode) to Port-A. RDY~ will be pulled high by the "Write" operation.
e. TSP53C30 will pull RDY~ low.
f. Read the data on Port-A. It will be an "FB" (request speech data).
g. From the time that RDY~ went from high to low, wait at least 32 clock periods but not more than 192 clock periods and then write the value for "C" to Port-A. RDY~ will go from low to high.
h. TSP53C30 will pull RDY~ low.
i. Read the data on Port-A. It will be an "FB" (request speech data).

j. From the time that RDY~ went from high to low, wait at least 32 clock periods but not more than 192 clock periods and then write the value for "B" to Port-A. RDY~ will go from low to high.
k. TSP53C30 will pull RDY~ low.
l. Read the data on Port-A. It will be an "FB" (request speech data).
m. From the time that RDY~ went from high to low, wait at least 32 clock periods but not more than 192 clock periods and then write the value for "A" to Port-A. RDY~ will go from low to high.
n. TSP53C30 will pull RDY~ low.
o. Read the data on Port-A. If it is an "FB" (request speech data) then go to (p). Otherwise it will be an "F7" (end of speech), stop.
p. From the time that RDY~ went from high to low, wait at least 32 clock periods but not more than 192 clock periods and then write the speech data to Port-A. RDY~ will go from low to high. Go to step (n).

3.2 5220/HOST MODE PROCEDURE

Speech data in the 5220 format is the same data that is used TSP5220C synthesizer. Speech data could be passed to the synthesizer either from a TSP6100 Vocabulary ROM (VROM) through a serial port or from a host processor's system memory through a parallel port. If the data was in the VROM it would be stored in the normal format. If the data was in the system memory it would be bit reversed, by bytes. To use this data with the TSP53C30 the data must be put back into the normal format. Appendix F is a listing of a Turbo Pascal program that performs this function.

Appendix B describes the data format for 5220 code. It also contains the lookup table that is used in the TSP53C30 to decode the data before putting it into the synthesizer.

The sequence of operation in the 5220/HOST mode is:

a. Cycle the INIT~ pin so that it makes a low-to-high transition.
b. TSP53C30 will pull RDY~ low.
c. Read the data on Port-A. It will be an "FE" (request operating mode command).
d. Write one of the following commands to Port-A:

command	speech speed	Input buffer length
06	normal	8 bytes
46	normal	16 bytes
86	normal	24 bytes
C6	normal	32 bytes
26	47% increase	8 bytes
66	47% increase	16 bytes
A6	47% increase	24 bytes
E6	47% increase	32 bytes

RDY~ will be pulled high by the "Write" operation.
e. TSP53C30 will pull RDY~ low.

f. Read the data on Port-A. If it is an "FB" (request speech data) then go to (g). Otherwise it will be an "F7" (end of speech), stop.
g. Write the speech data to Port-A.
RDY~ will go from low to high.
Go to step (e).

3.3 D6/HOST MODE PROCEDURE

Speech data in the D6 format is similar to the 5220 format except that some of the speech parameters have been given a greater resolution. See Appendix C for the data format and the lookup table that is used to decode this data.

The sequence of operation in the D6/HOST mode is:

a. Cycle the INIT~ pin so that it makes a low-to-high transition.
b. TSP53C30 will pull RDY~ low.
c. Read the data on Port-A. It will be an "FE" (request operating mode command).
d. Write one of the following commands to Port-A;

command	speech speed	Input buffer length
04	normal	8 bytes
44	normal	16 bytes
84	normal	24 bytes
C4	normal	32 bytes
24	47% increase	8 bytes
64	47% increase	16 bytes
A4	47% increase	24 bytes
E4	47% increase	32 bytes

RDY~ will be pulled high by the "Write" operation.
e. TSP53C30 will pull RDY~ low.
f. Read the data on Port-A. If it is an "FB" (request speech data) then go to (g). Otherwise it will be an "F7" (end of speech), stop.
g. Write the speech data to Port-A.
RDY~ will go from low to high.
Go to step (e).

3.4 UNPACKED/HOST MODE PROCEDURE

The input data buffer banks are preset to the number of bytes in a frame of speech data. A frame of data consists of 15 to 21 bytes, determined by the Operating Command word. A full frame has the following data:

byte number	data
1	Frame length
2	Pitch
* 3	S / Fractional Pitch
4	Energy
5	Fractional Energy
6	K1 Parameter
7	K2 Parameter
8	K3 Parameter
9	K4 Parameter
10	K5 Parameter
11	K6 Parameter
12	K7 Parameter
13	K8 Parameter
14	K9 Parameter
15	K10 Parameter
16	Fractional K1 Parameter
17	Fractional K2 Parameter
18	Fractional K3 Parameter
19	Fractional K4 Parameter
20	Fractional K5 Parameter
21	Fractional K6 Parameter

* The most significant bit is the stop code. The four least significant bits is the fractional pitch data.

The sequence of operation in the UNPACKED/HOST mode is:

a. Cycle the INIT~ pin so that it makes a low-to-high transition.
b. TSP53C30 will pull RDY~ low.
c. Read the data on Port-A. It will be an "FE" (request operating mode command).
d. Write one of the following commands to Port-A;

command	frame length	fractional reflection coefficients
02	15 bytes	none
22	16 bytes	K1
42	17 bytes	K1, K2
62	18 bytes	K1, K2, K3
82	19 bytes	K1, K2, K3, K4
A2	20 bytes	K1, K2, K3, K4, K5
C2	21 bytes	K1, K2, K3, K4, K5, K6

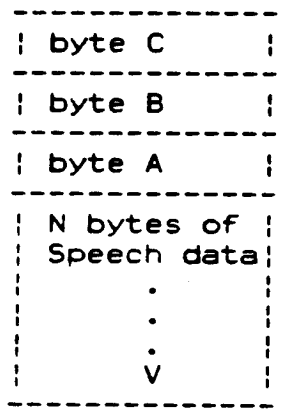
RDY~ will be pulled high by the "Write" operation.

e. TSP53C30 will pull RDY~ low.

f. Read the data on Port-A. If it is an "FB" (request speech data) then go to (g). Otherwise it will be an "F7" (end of speech), stop.
g. Write the speech data to Port-A.
RDY~ will go from low to high.
Go to step (e).

3.5 PCM/VROM MODE PROCEDURE, DIRECT OR INDIRECT ADDRESSING

The speech data is stored in a TSP60C20 VROM in two's complement data format. The data is preceded by three bytes that specify the number of data bytes. The format for these three bytes is:



N is equal to:

$$(65{,}281 \times C) + (256 \times B) + A + 3 = N$$

Where;

C --- The first byte in the data file
B --- The second byte in the data file
A --- The third byte in the data file
N --- The number of PCM data bytes that are being defined by C, B, and A.

The data can be accessed by writing the PCM/VROM operation command to the TSP53C30 and then providing the direct or indirect address for the speech data in the VROM. The sequence of operation is:

a. Cycle the INIT~ pin so that it makes a low-to-high transition.
b. TSP53C30 will pull RDY~ low.
c. Read the data on Port-A. It will be an "FE" (request operating mode command).
d. Write one of the following commands to Port-A;

command	operation
01	Direct Addressing
09	Indirect Addressing

RDY~ will will be pulled high by the "Write" operation.
e. TSP53C30 will pull RDY~ low.

f. Read the data on Port-A. It will be an "FD" (request speech data address).
g. From the time that RDY~ went from high to low [in step (e)], wait at least 32 clock periods and then write the most significant byte of the address to Port-A. RDY~ will go from low to high.
h. TSP53C30 will pull RDY~ low.
i. Read the data on Port-A. It will be an "FD" (request speech data address).
j. From the time that RDY~ went from high to low [in step (h)], wait at least 32 clock periods and then write the least significant byte of the address to Port-A. RDY~ will go from low to high.
k. When the TSP53C30 processes the number of speech data bytes defined by the first three bytes in the data file RDY~ will go from high to low.
l. Read the data on Port-A. It will be an "F7" (end of speech). The TSP53C30 will power down after the "F7" is read.

3.6 5220/VROM MODE PROCEDURE, DIRECT OR INDIRECT ADDRESSING

The sequence of operation in the 5220/VROM mode is:

a. Cycle the INIT~ pin so that it makes a low-to-high transition.
b. TSP53C30 will pull RDY~ low.
c. Read the data on Port-A. It will be an "FE" (request operating mode command).
d. Write one of the following commands to Port-A:

command	speech speed	addressing
07	normal	direct
0F	normal	indirect
27	47% increase	direct
2F	47% increase	indirect

RDY~ will be pulled high by "Write" operation.
e. TSP53C30 will pull RDY~ low.
f. Read the data on Port-A. It will be an "FD" (request speech data address).
g. From the time that RDY~ went from high to low [in step (e)], wait at least 32 clock periods and then write the most significant byte of the address to Port-A. RDY~ will go from low to high.
h. TSP53C30 will pull RDY~ low.
i. Read the data on Port-A. It will be an "FD" (request speech data address).
j. From the time that RDY~ went from high to low [in step (h)], wait at least 32 clock periods and then write the least significant byte of the address to Port-A. RDY~ will go from low to high.
k. When the TSP53C30 detects a stop code in the speech data RDY~ will go from high to low.

l. Read the data on Port-A. It will be an "F7" (end of speech). The TSP53C30 will power down after the "F7" is read.

3.7 D6/VROM MODE PROCEDURE, DIRECT OR INDIRECT ADDRESSING

The sequence of operation in the D6/VROM mode is:

a. Cycle the INIT~ pin so that it makes a low-to-high transition.
b. TSP53C30 will pull RDY~ low.
c. Read the data on Port-A. It will be an "FE" (request operating mode command).
d. Write one of the following commands to Port-A;

command	speech speed	addressing
05	normal	direct
0D	normal	indirect
25	47% increase	direct
2D	47% increase	indirect

RDY~ will be pulled high by the "Write" operation.
e. TSP53C30 will pull RDY~ low.
f. Read the data on Port-A. It will be an "FD" (request speech data address).
g. From the time that RDY~ went from high to low [in step (e)], wait at least 32 clock periods and then write the most significant byte of the address to Port-A. RDY~ will go from low to high.
h. TSP53C30 will pull RDY~ low.
i. Read the data on Port-A. It will be an "FD" (request speech data address).
j. From the time that RDY~ went from high to low [in step (h)], wait at least 32 clock periods and then write the least significant byte of the address to Port-A. RDY~ will go from low to high.
k. When the TSP53C30 detects a stop code in the speech data RDY~ will go from high to low.
l. Read the data on Port-A. It will be an "F7" (end of speech). The TSP53C30 will power down after the "F7" is read.

3.8 UNPACKED/VROM MODE PROCEDURE, DIRECT OR INDIRECT ADDRESSING

The sequence of operation in the UNPACKED/VROM mode is:

a. Cycle the INIT~ pin so that it makes a low-to-high transition.
b. TSP53C30 will pull RDY~ low.
c. Read the data on Port-A. It will be an "FE" (request operating mode command).

d. Write one of the following commands to Port-A;

command	addressing
03	direct
0B	indirect

RDY~ will be pulled high by the "Write" operation.

e. TSP53C30 will pull RDY~ low.
f. Read the data on Port-A. It will be an "FD" (request speech data address).
g. From the time that RDY~ went from high to low [in step (e)], wait at least 32 clock periods and then write the most significant byte of the address to Port-A. RDY~ will go from low to high.
h. TSP53C30 will pull RDY~ low.
i. Read the data on Port-A. It will be an "FD" (request speech data address).
j. From the time that RDY~ went from high to low [in step (h)], wait at least 32 clock periods and then write the least significant byte of the address to Port-A. RDY~ will go from low to high.
k. When the TSP53C30 detects a stop code in the speech data RDY~ will go from high to low.
l. Read the data on Port-A. It will be an "F7" (end of speech). The TSP53C30 will power down after the "F7" is read.

4.0 Electrical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range

Supply voltage, V_{DD} . . . . . −0.3 V to 7 V
Input voltage, V_I . . . . . −0.3 V to V_{DD} + 0.3 V
Output voltage, V_O . . . . . −0.3 V to V_{DD} + 0.3 V
Storage temperature range . . . . . −30 °C to 125 °C
All voltages are with respect to V_{SS}.

Recommended Operating Conditions — DC

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{DD}*			4	5	6	V
T_A	Operating free-air temperature		0		70	°C
V_{IH}	V_{DD} = 4 V		3		4	V
	V_{DD} = 5 V		3.8		5	
	V_{DD} = 6 V		4.5		6	
V_{IL}	V_{DD} = 4 V				1	V
	V_{DD} = 5 V				1.2	
	V_{DD} = 6 V				1.5	
V_L	V_{DD} = 5 V,	R_L = 50 Ω	1.9	2.8		V
	V_{DD} = 5 V,	R_L = 100 Ω	2.9	3.6		
	V_{DD} = 4 V,	R_L = 50 Ω	1.3	2		
	V_{DD} = 4 V,	R_L = 100 Ω	2	2.7		
Output power D/A	V_{DD} = 5 V,	R_L = 50 Ω	72	157		mW
	V_{DD} = 5 V,	R_L = 100 Ω	84	130		
	V_{DD} = 4 V,	R_L = 50 Ω	34	80		
	V_{DD} = 4 V,	R_L = 100 Ω	40	73		
Pullup Res	V_{DD} = 5 (when programmed)		~~30~~ 37	~~36~~ 50	~~36~~ 100	kΩ

*Unless otherwise noted, all voltages are with respect to V_{SS}.

Recommended Operating Conditions — AC

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_r	V_{DD} = 5 V, PA,B,D into 100 pF 10% to 90%			150	ns
t_f	V_{DD} = 5 V, PA,B,D into 100 pF 10% to 90%			100	ns
f_{osc}	Speech Sample Rate = 10 kHz		3.84		MHz
	Speech Sample Rate = 8 kHz		3.07		

Electrical Characteristics over Recommended Operating Free-Air Temperature Range

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	V_{DD} = 5 V Standby mode = SETOFF executed or $\overline{INIT}$ high, no pullup resistor on $\overline{INIT}$, all port pins are open.		10	50	μA
	V_{DD} = 5 V Operating mode = $\overline{INIT}$ high and SETOFF not executed, DA pins are open.		1.5	3	mA
V_{OH}	V_{DD} = 5 V, I_{OH} = 0.3 mA	4.7	4.85		V
	I_{OH} = 1.2 mA	4	4.5		
V_{OL}	V_{DD} = 5 V, I_{OL} = 1.7 mA		0.3	0.4	V
I_I	Input current			5.0	μA
I_{OH}	V_{DD} = 4 V, V_{OH} = 3.5 V	0.3	0.8		mA
	V_{DD} = 5 V, V_{OH} = 4.5 V	0.6	1.2		
	V_{DD} = 6 V, V_{OH} = 5.5 V	0.8	1.5		
I_{OL}	V_{DD} = 4 V, V_{OL} = 0.4 V	1.2	1.8		mA
	V_{DD} = 5 V, V_{OL} = 0.4 V	1.7	2.4		
	V_{DD} = 6 V, V_{OL} = 0.4 V	2	2.8		
r_o	V_{DD} = 5 V, DA1 and DA2 pins		50		Ω

Oscillator

The oscillator pins OSC1 and OSC2 are provided for either a crystal or ceramic resonator connection in the typical phase shift oscillator connection. The recommended value for circuit components C1 and C2 are shown.

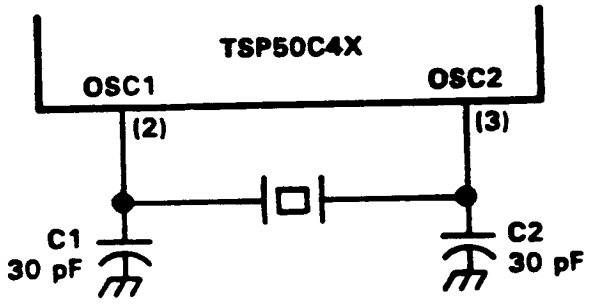


Figure 4-1 Typical Phase Shift Oscillator Connection

Direct Speaker Driver

The analog buffers at DA1 and DA2 are designed to directly drive a 50- to 100-Ω speaker with approximately 120 to 150 mW of peak power. Average power is considerably below this figure. The reduction in power is caused by the nature of speech. The effective analog output impedance at 5 V is typically 50 Ω for output currents less than 60 mA. For output currents more than 60 mA, the DAC buffers act as current sources. The outputs can also be used to drive transistors or operational amplifiers.

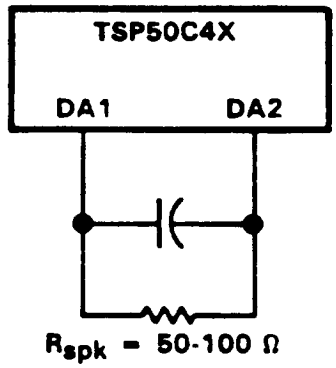


Figure 4–2 Typical Direct Speaker Drive Connection

Timing Requirements

Table 4-1 Initialization Timing

	CONDITION	MIN	MAX	UNIT
t_W	TSP53C30 in the standby mode DUE TO INTERNAL PROGRAM EXECUTING SETOFF	10		ns
	$\overline{INIT}$ pulsed low while the TSP53C30 is active	*		

*One oscillator clock period.

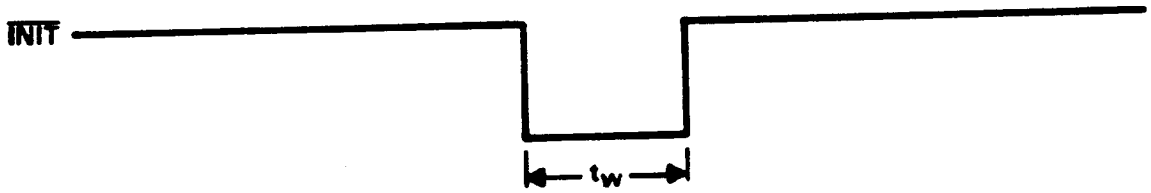


Figure 4-3 Initialization Timing

Table 4-2 Timing Requirements

	SAMPLE RATE		UNIT
	10 kHz NOM	8 kHz NOM	
Sample period	100	125	μs
ROM clock rate	240	192	kHz
ROM clock period	4.17	5.20	μs
Oscillator rate	3.84	3.07	MHz
Oscillator period	260	3.25	ns

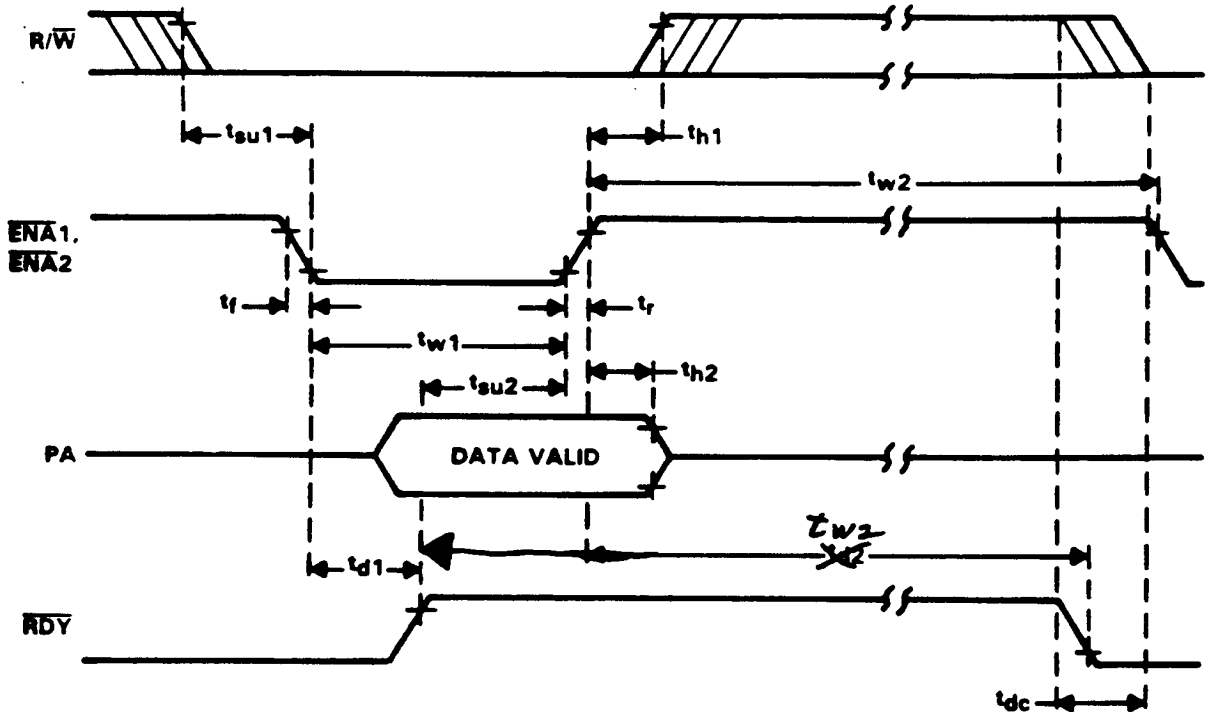


Figure 4-4 Write Timing Diagram

Table 4-3 Write Timing Requirements (see Figure 4-4)

PARAMETER		MIN	MAX	UNIT
t_{su1}	Setup time, R/$\overline{W}$ before $\overline{ENA1}$↓ or $\overline{ENA2}$↓	80		ns
t_{su2}	Setup time, data valid before $\overline{ENA1}$↑ or $\overline{ENA2}$↑	100		ns
t_{h1}	Hold time, R/$\overline{W}$ after $\overline{ENA1}$↓ or $\overline{ENA2}$↓	40		ns
t_{h2}	Hold time, data valid after $\overline{ENA1}$↑ or $\overline{ENA2}$↑	40		ns
t_{w1}	Pulse duration, $\overline{ENA1}$ or $\overline{ENA2}$ low	200		ns
t_{dc}	Cycle delay time	32		CLK cycles
t_r	Rise time, $\overline{ENA1}$ or $\overline{ENA2}$		50	ns
t_f	Fall time, $\overline{ENA1}$ or $\overline{ENA2}$		50	ns
t_{d1}	Delay time from $\overline{ENA1}$ low or $\overline{ENA2}$ low to $\overline{RDY}$ high		250	ns
~~t_{w2}~~ ~~t_{DC}~~	~~Delay time from $\overline{ENA1}$ high or $\overline{ENA2}$ high to $\overline{RDY}$ low~~ $\overline{RDY}$ PULSE DURATION		TO BE DETERMINED ~~Program Dependent~~	

NOTE: $\overline{ENA1}$ applies to PA4 through PA7, and $\overline{ENA2}$ applies to PA0 through PA3.

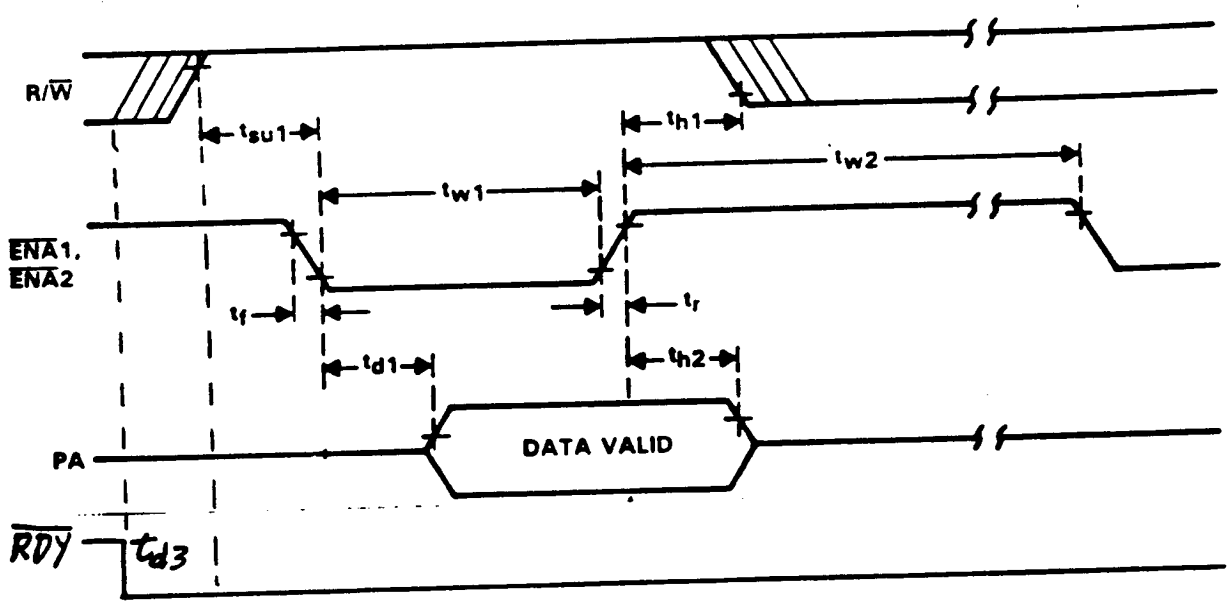


Figure 4-5 Read Timing Diagram

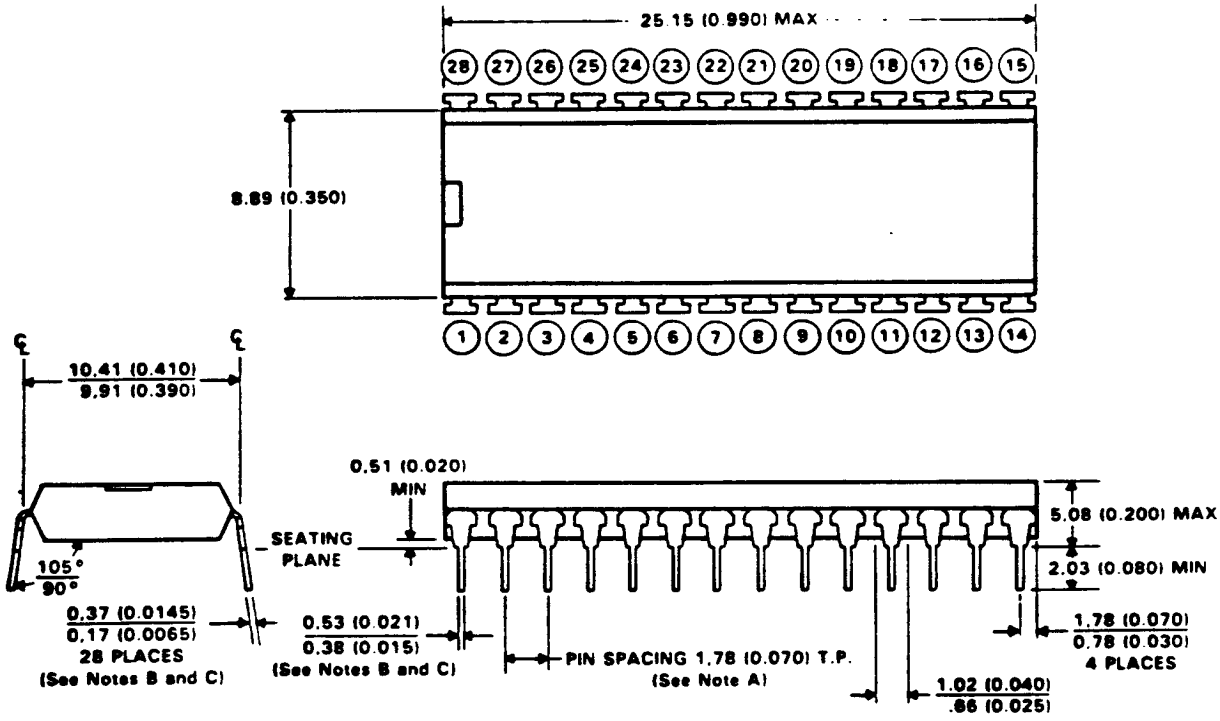
Table 4-4 Read Timing Requirements (see Figure 4-5)

PARAMETER		MIN	MAX	UNIT
t_{su1}	Setup time, R/W before ENA1↓ or ENA2↓	80		ns
t_{h1}	Hold time, R/W after ENA1↑ or ENA2↑	40		ns
t_{h2}	Hold time, data valid after ENA1↑ or ENA2↑	100		ns
t_{w1}	Pulse duration, ENA1 or ENA2 low	200		ns
t_{w2}	Pulse duration, ENA1 or ENA2 high	2		μs
t_r	Rise time, ENA1 or ENA2		50	ns
t_f	Fall time, ENA1 or ENA2		50	ns
t_{d1}	Delay time from ENA1 low or ENA2 low to data valid		250	ns
t_{d2}	Delay time from ENA1 low or ENA2 low to IRT high		250	ns
t_{d3}	Delay time from ~~ENA1 high or ENA2 high to RDY low~~ RDY LOW TO R/W HIGH		DETERMINED ~~Program Dependent~~ BY HOST PROCESSOR	

IRT NOT USED

NOTE: ENA1 applies to PA4 through PA7, and ENA2 applies to PA0 through PA3.

5.0 Mechanical Data



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

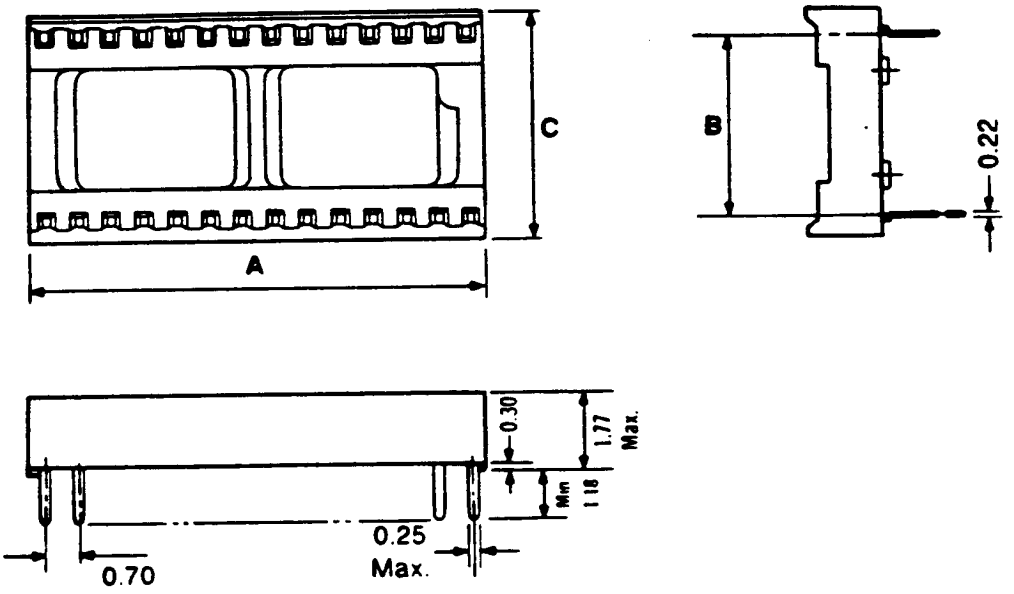
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

Figure 5-1 TSP53C30 ~~TSP50C41 and TCP50C43~~ 28-Pin NF* Plastic Package
0.070" Pin Center Spacing, 0.400" Pin Row Spacing

* THE NF PACKAGE HAS ALSO BEEN DESIGNATED N2.

6.0 IC Sockets

Texas Instruments lines of off-the-shelf interconnection products are designed specifically to meet the performance needs of volume commercial applications. They provide both the economy of a standard product line and performance features developed after many years experience with custom designs.



Positions	A max. Length	B ± .005 Row to Row	C max. Width	PART NUMBER
28	.985 (25,02)	.400 (10,16)	.512 (13,00)	C4S28-02
40	1.405 (35,69)	.600 (15,24)	.708 (17,98)	C4S40-02

Dimension In Parentheses Are Metric

Figure 6-1 Shrink Package C4S Series 28 and 40 Positions

Additional information including pricing and delivery quotations may be obtained from your nearest TI Distributor, TI Representative, or:

Texas Instruments Incorporated
Connector Systems Department
MS 14-3
Attleboro, Massachusetts 02703
Telephone: ~~(617)~~ 699-3800 (508)
TELEX: ABORA927708