SGS-THOMSON MICROELECTRONICS

T-58-11-31

L4970

S G S-THOMSON 30E D

10A SWITCHING REGULATOR

ADVANCE DATA

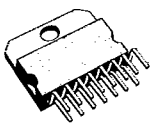
- 10A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ±2% ON CHIP REFERENCE
- RESET AND P. FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4970 include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

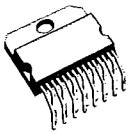
MULTIPOWER BCD TECHNOLOGY

Multiwatt 15 ®
(15-lead)

Vertical



Horizontal

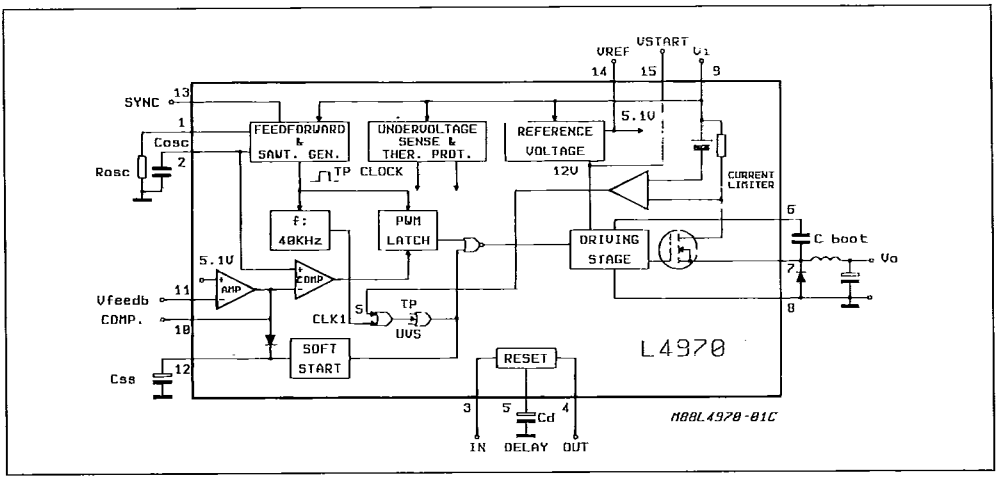


ORDER CODE : L4970 (Vertical)
L4970HT (Horizontal)

DESCRIPTION

The L4970 is a stepdown monolithic power switching regulator delivering 10A at a voltage variable from 5.1 to 40V.

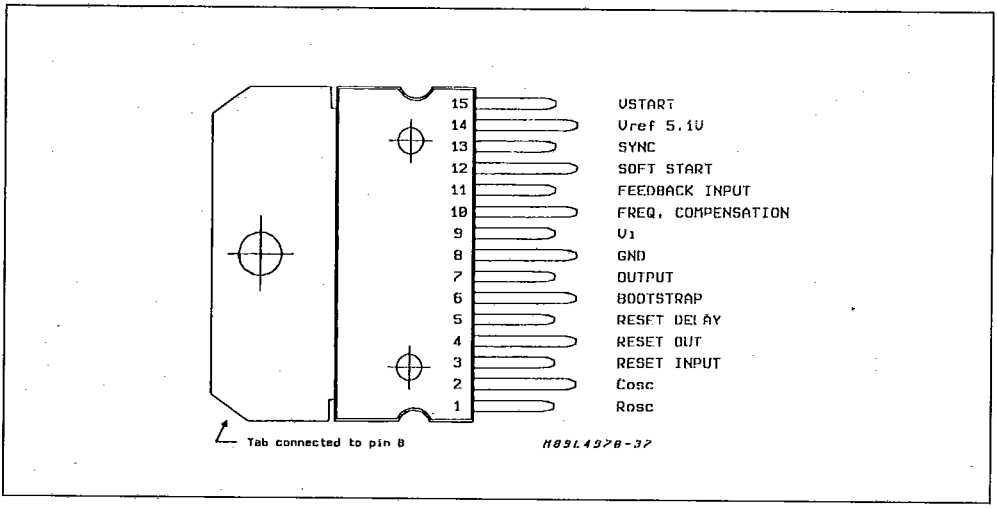
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	– 1 – 7	V V
I_7	Max Output Current	Internally limited	
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{12}	Input Voltage at Pins 3, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{11}, V_{13}	Input Voltage at Pin 5, 10, 11, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	1	mA
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120°C	30	W
T_j, T_{stg}	Junction and Storage Temperature	– 40 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

Rth j–case	Thermal Resistance Junction–case	Max	1	°C/W
Rth j–amb	Thermal Resistance Junction–ambient	Max	35	

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 15 with an external 30KΩ resistor when power fail signal not required.
4	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
7	OUTPUT	Regulator Output
8	GROUND	Common Ground Terminal
9	SUPPLY VOLTAGE	Unregulated Input Voltage
10	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
12	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant.
13	SYNC INPUT	Multiple L4970's are synchronized by connecting pin 13 inputs togheter or via an external syncr. pulse.
14	V_{ref}	5.1V_{ref} Device Reference Voltage
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage

CIRCUIT OPERATION (refer to the block diagram).

The L4970 is a 10A monolithic stepdown switching regulator realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 10A at an output voltage adjustable from 5.1V to 40V, and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistor and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysterysis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysterysis prevents instabilities.

An external bootstrap capacitor charged to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50nS. Due to the fast commutation switching frequencies upto 500kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing

Figure 1 : Feedforward Waveform.

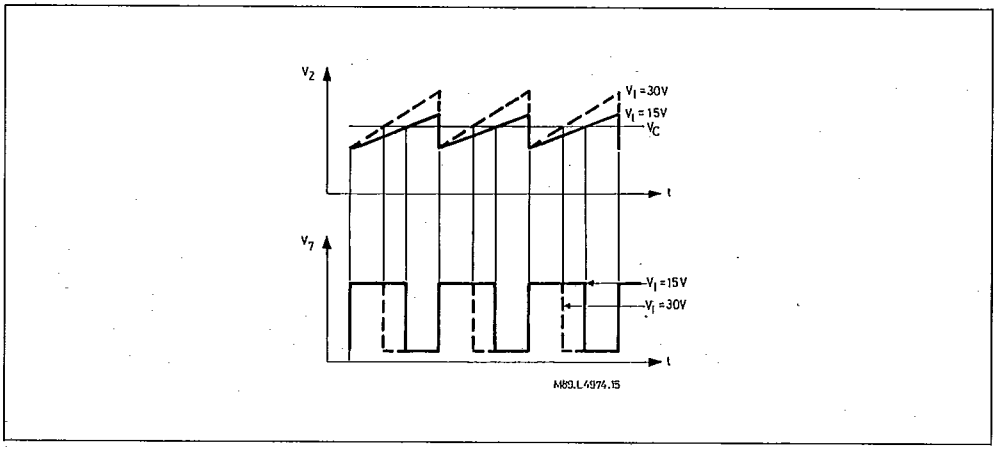


Figure 2 : Soft Start Function.

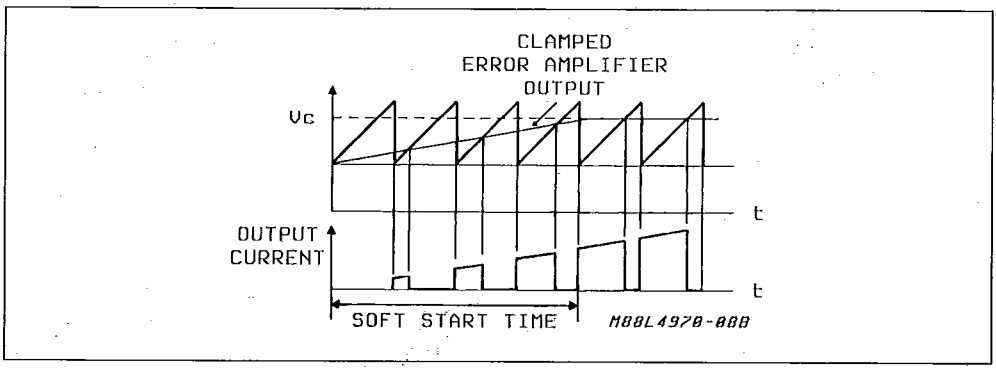
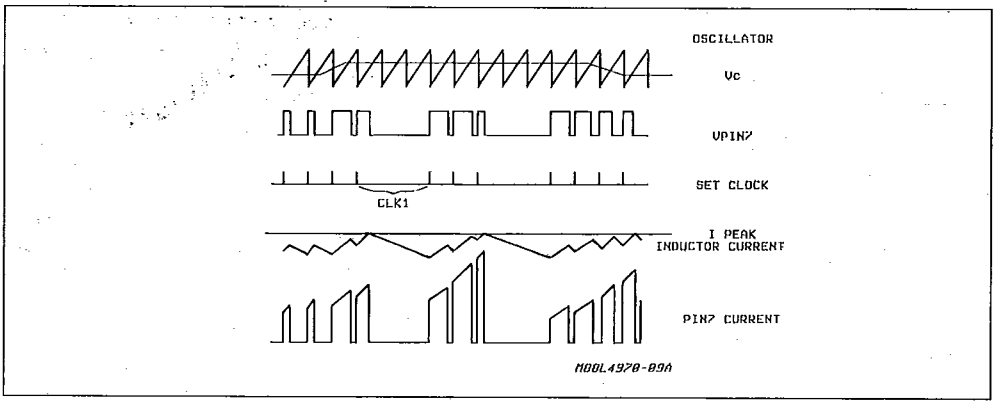


Figure 3 : Limiting Current Function.



the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator in order to generate fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy enviroments. The gain and stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor Css and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse from an internal 40kHz oscillator will reset the flip flop and the power DMOS will again conduct. This current protection method ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency in this condition to 40kHz.

The Reset and Power fail circuit (fig. 4) generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal is generated with a delay time programmed by a external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V the reset output goes low immediately. The reset output is an open collector drain.

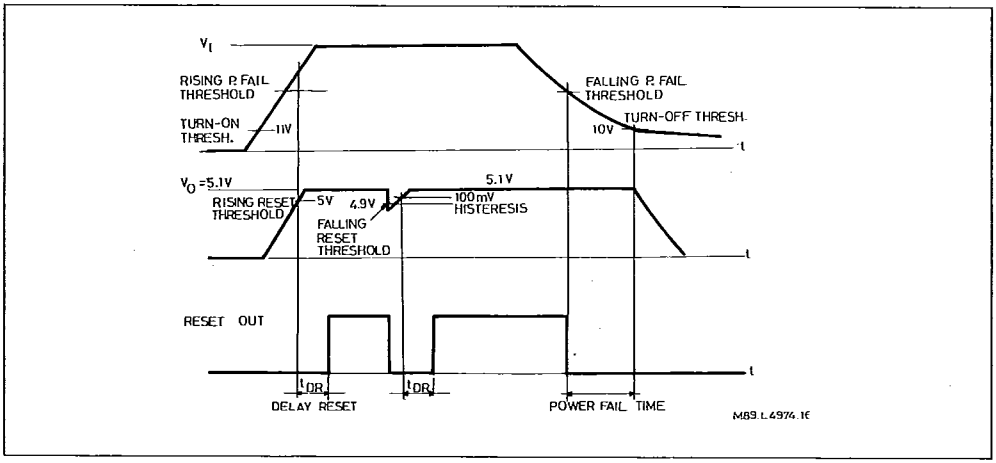
Fig. 4A shows the case when the supply voltage is higher than the threshold but the output voltage is not yet 5V.

Fig. 4B shows the case when the output is 5.1V but the supply voltage is not yet higher than the fixed threshold.

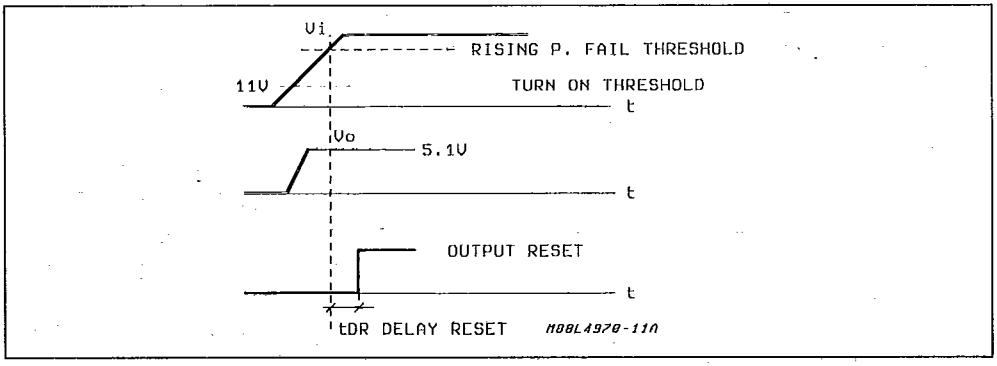
The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has an hysterysis to prevent unstable conditions.

Figure 4 : Reset and Power Fail Functions.

A



B



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 15KΩ, C_9 = 2.2nF, f_{sw} = 200KHz typ., unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_i	Input Volt. Range (pin 9)	V_o = V_{ref} to 40V I_o = 10A	15		50	V	5
V_o	Output Voltage	V_i = 15V to 50V I_o = 5A ; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 2A ; V_o = V_{ref}		12	30	mV	5
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 3A to 6A I_o = 2A to 10A		 10 20	 30 50	 mV mV	5
V_d	Dropout Voltage between Pin 9 and 7	I_o = 5A I_o = 10A		0.55 1.1	0.8 1.6	V V	5
I_{7L}	Max Limiting Current	V_i = 15V to 50V V_o = V_{ref} to 40V	11	12.5	14	A	5
Efficiency		I_o = 5A V_o = V_{ref} V_o = 12V	80	85 92		5 % %	5
		I_o = 10A V_o = V_{ref} V_o = 12V	75	80 87		5 %	5
SVR	Supply Voltage Ripple Reject.	V_i = 2VRMS ; I_o = 5A f = 100Hz ; V_o = Vref	56	60		dB	5
f	Switching Freq.		180	200	220	KHz	5
$\Delta f/\Delta V_i$	Volt. Stability of Switching Freq.	V_i = 15V to 45V		2	6	%	5
$\Delta f/T_j$	Temp. Stablity of Switch. Freq.	T_j = 0 to 125°C		1		%	5
f_{max}	Max. Operating Switch. Freq.	V_o = V_{ref} ; R_4 = 9.1KΩ I_o = 10A ; C_9 = 1.2nF	500			KHz	5

ELECTRICAL CHARACTERISTICS (continued)

V_{REF} SECTION (pin 14)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{REF}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{REF}	Line Regulation	V_i = 15V to 50V V_{12} = 0		10	25	mV	7
ΔV_{REF}	Load Regulation	I_{REF} = 0 to 3mA		20	40	mV	7
$\Delta V_{REF}/\Delta T$	Average Temp. Coeff. Ref. Voltage	T_j = 0°C to 125°C		0.4		mV/C	7
I_{REF}	Short Circuit Curr. Limit	V_{REF} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{ref}	Reference Voltage	P_{12} = 0V	11.4	12	12.6	V	7
ΔV_{ref}	Line Regulation	P_{12} = 0V ; V_i = 15 to 50V		0.4	1	V	7
ΔV_{ref}	Load Regulation	I_{ref} = 0 to 1mA P_{12} = 0V		50	200	mV	7
I_{ref}	Short Circuit Current Limit	P_{12} = 0V ; P_{15} = 0V		80		mA	7

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{9on}	Turn–on Thresh.		10	11	12	V	7A
V_{9Hyst}	Turn–off Hyster.			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0 ; S1 = D ; S2 = C ; S4 = A		10	16	mA	7A
I_{9OQ}	Operating Quiescent Curr.	V_{12} = 0		16	20	mA	7A
I_{7L}	Out Leak Current	V_i = 55V ; S3 = A ; V_{12} = 0V			2	mA	7A

SOFT START (pin 12)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{12}	Soft Start Source Current	V_{12} = 3V ; V_{11} = 0V	70	100	130	µA	7B
V_{12s}	Output Saturation Voltage	I_{12s} = 20mA ; V_9 = 10V			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{10H}	High Level out Voltage	I_{10} = – 50µA ; S2 = A P_{11} = 0V ; S1 = C	6			V	7C
V_{10L}	Low Level out Voltage	I_{10} = 50µA ; S2 = A P_{11} = 6V ; S1 = C			0.7	V	7C
I_{11}	Input Bias Current	V_{11} = 5 ; S1 = B ; R_S = 10K		2	10	uA	7C
VOS	Input off Voltage	P_{11} = Vos ; R_s = 50Ω ; S1 = A		2	10	mV	7C
G_V	DC Open Loop Gain	P_{VCM} = 4V ; R_S = 50Ω ; S1 = A	60			dB	7C
SVR	Supply Volt. Rej.	15 < Vi < 50V	60	80		dB	7C

ELECTRICAL CHARACTERISTICS (continued)

RAMP GENERATOR (pin 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
	Ramp Valley			1.5		V	7A
	Ramp Peak	V_i = 15V V_i = 45V		2.5 5.5		V V	7A
	Min Ramp Current	S1 = A ; I1 = 100µA		270	300	µA	7A
	Max Ramp Current	S1 = A ; I1 = 1mA	2.4	2.7		mA	7A

SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SYNC	Low Input Voltage	V_i = 15V to 50V	– 0.3		0.9	V	
SYNC	High Input Voltage	V_{12} = 0	3.5		5.5	V	
$-I_{13L}$	Sync Input Current with Low Input Voltage	V_{13} = 0.9V			0.4	mA	
$-I_{13H}$	Input Current with High Input Voltage	V_{13} = 3.5V			1.5	mA	
SYNC	Delay			50		ns	
	Output Amplitude		4	5		V	
	Output Pulse Width	V_{thr} = 2.5V	0.3	0.5	0.8	µsec.	

RESET AND P. FAIL FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50V S1 = B	Vref – 120	Vref – 100	Vref – 80	V mV	7D
V_{11F}	Falling Threshold Voltage (pin 11)	V_i = 15 to 50V S1 = B	4.77	Vref – 200	Vref – 160	V mV	7D
V_{5H}	Delay High Threshold Voltage	S1 = B	5	5.1	5.2	V	7D
V_{5L}	Delay Low Threshold Voltage	S1 = B	1	1.1	1.2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5.3V ; V_5 = 3V S1 = A	40	55	70	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7V ; V_5 = 3V S1 = A	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15mA ; S2 = B			0.4	V	7D
I_4	Output Leak Current	V_4 = 50V ; S2 = A			100	µA	7D
V_{3R}	Rising Threshold Voltage		5	5.1	5.2	V	7D
	Hysteresis		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5 : Test and Application Circuit.

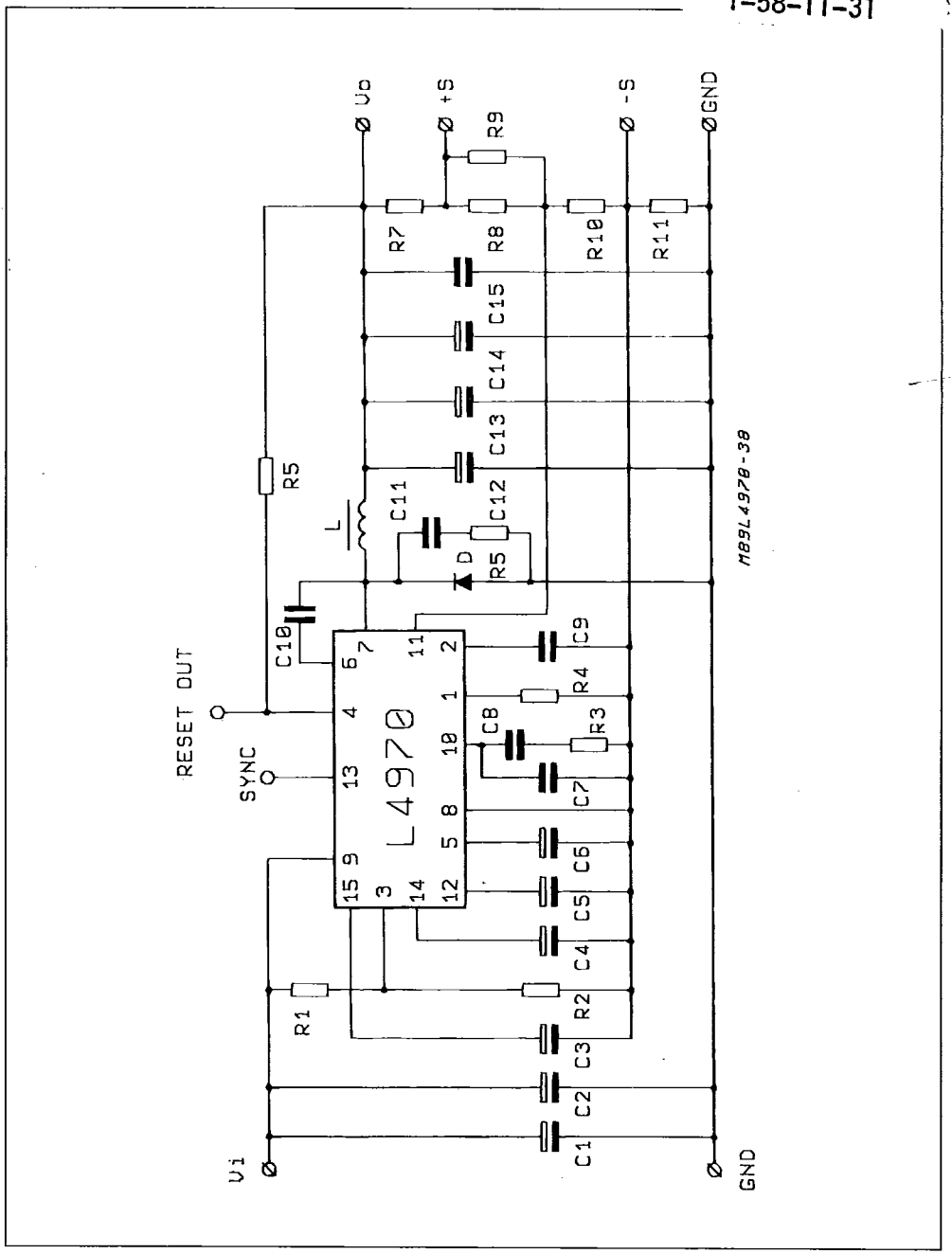
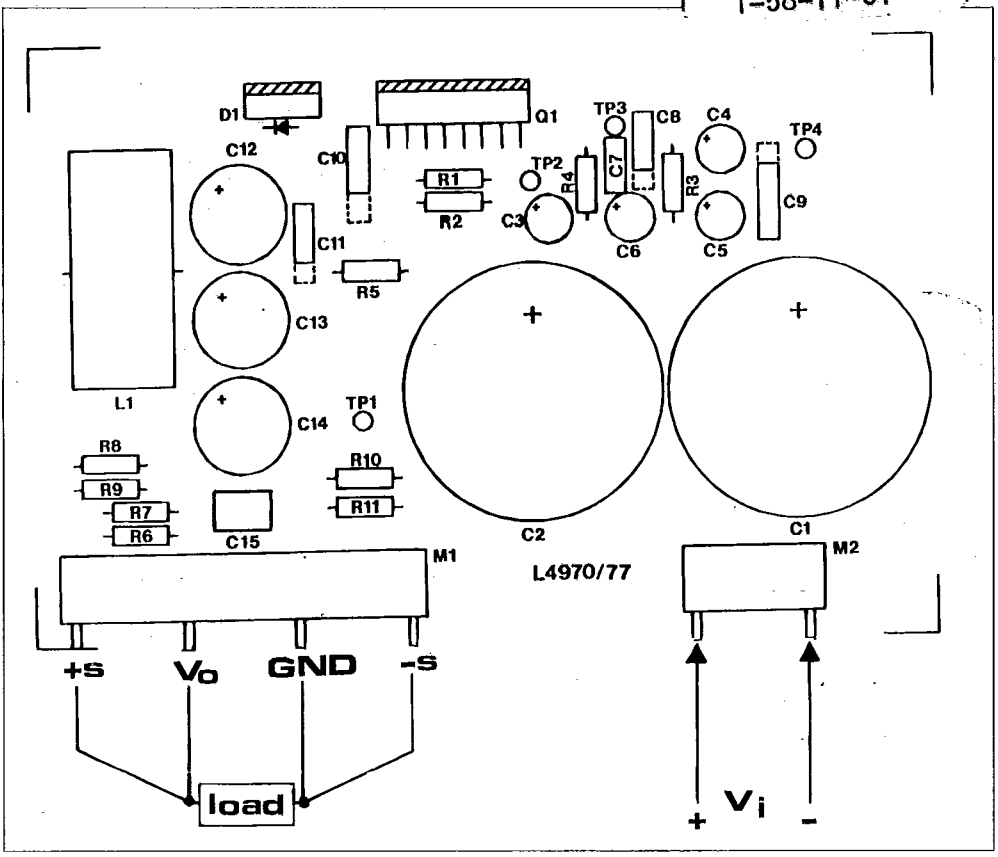


Figure 6 : Component Layout of Figure 5 (1:1 scale).



PART LISTS

R_1 = 30KΩ	*C_1, C_2 = 3300µF 63 V_L EYF (ROE)
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 22KΩ	C_7 = 390pF
R_4 = 15KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22KΩ 0.5W	C_9 = 2.2nF KP1830
R_6 = 4K7	C_{10} = 0.1µF MKT
R_7 = 10KΩ	C_{11} = 2.2nF MP 1830
R_8 = see table A	**C_{12}, C_{13}, C_{14} = 220µF 40 V_L EKR (ROE)
R_9 = OPTION	C_{15} = 1µF Film
R_{10} = 4K7	
R_{11} = 10Ω	
D = SBP 1660T	(or 16A/60V equivalent)
L = 40µH	core 58071 MAGNETICS 27 TURNS Ø 1,3mm (AWG 16) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability

** 3 capacitors in parallel to reduce total output ESR.

Table A.

V_0	R_{10}	R_8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	4.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Figure 7 : DC Test Circuits.

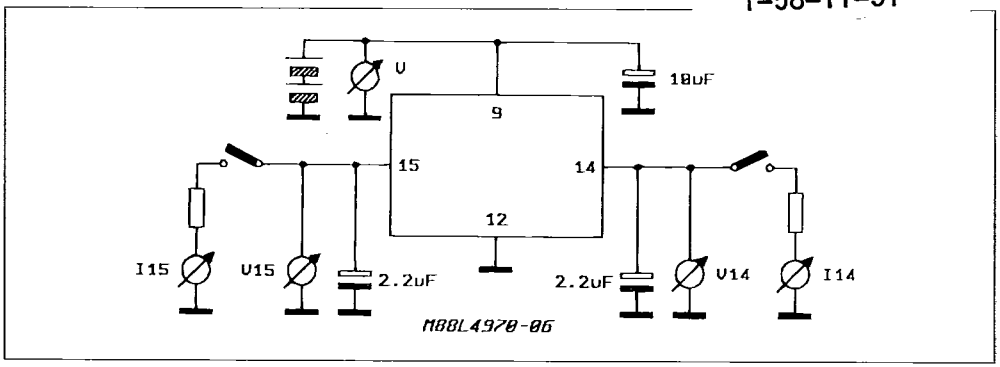


Figure 7A.

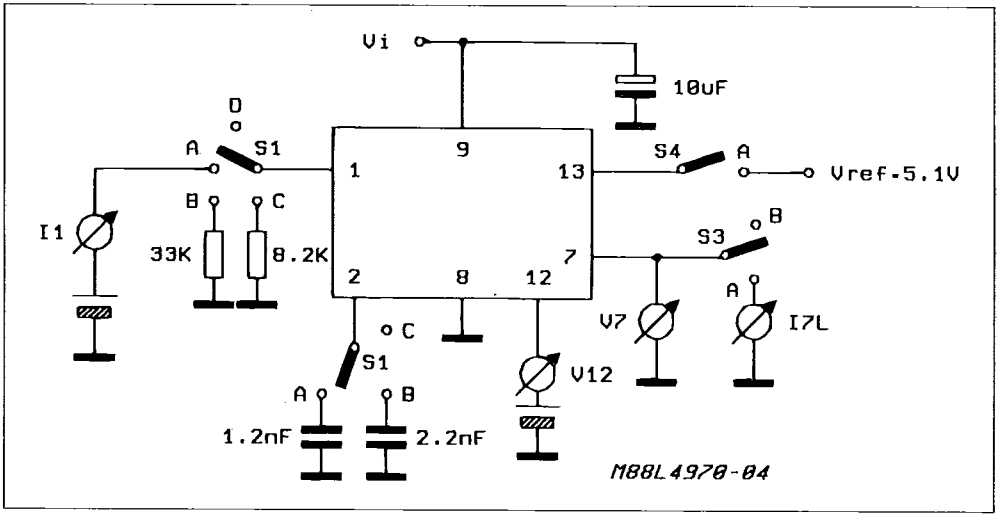


Figure 7B.

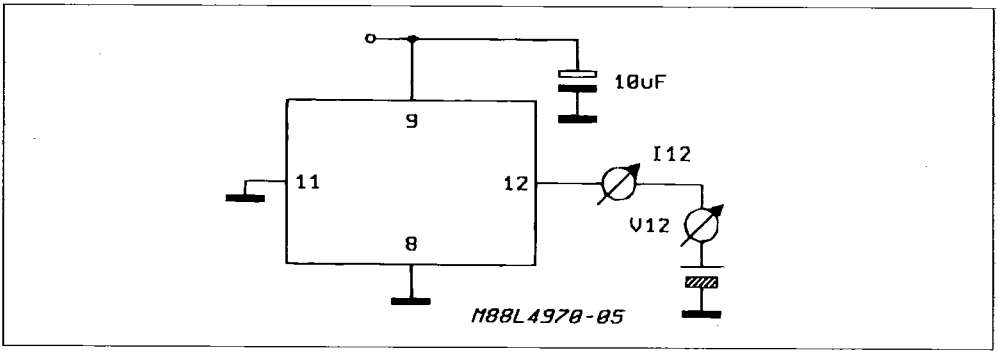


Figure 7C.

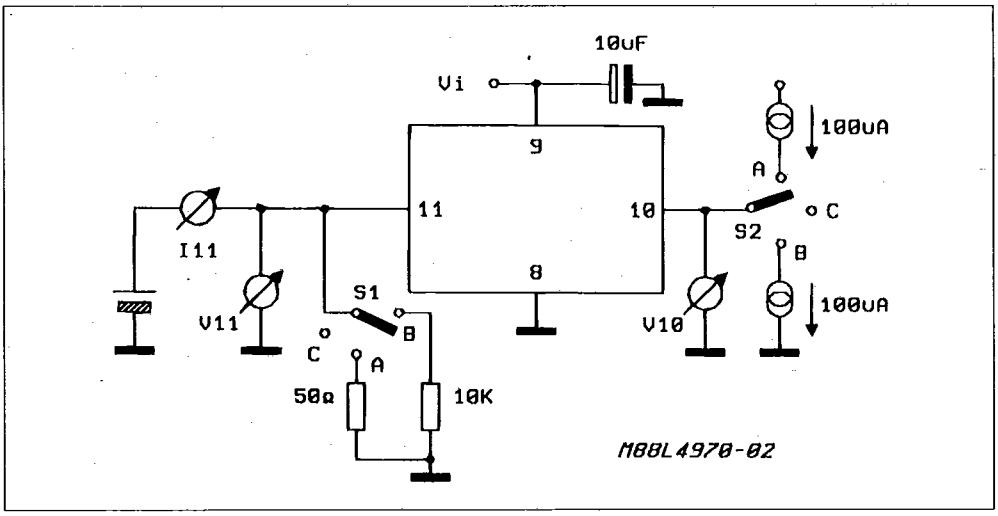


Figure 7D.

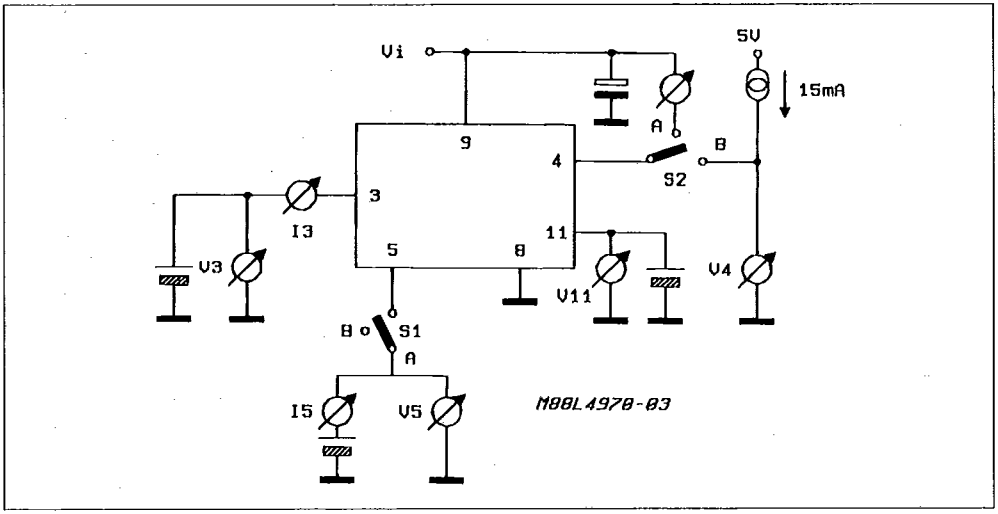


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0 % duty cycle - see fig. 7A).

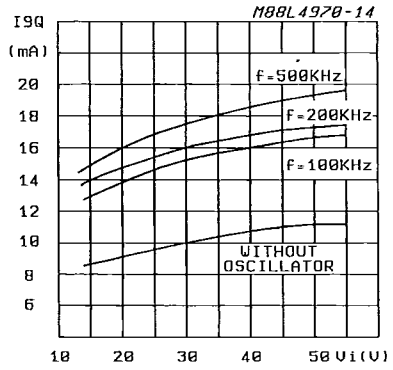


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0 % duty cycle).

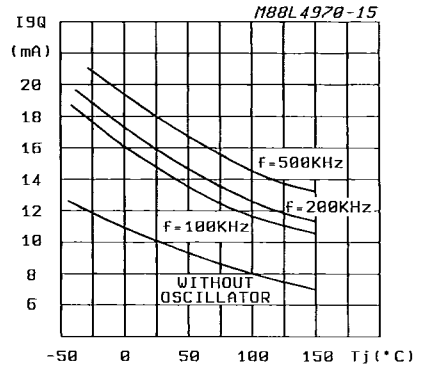


Figure 10 : Quiescent Drain Current vs. Duty Cycle.

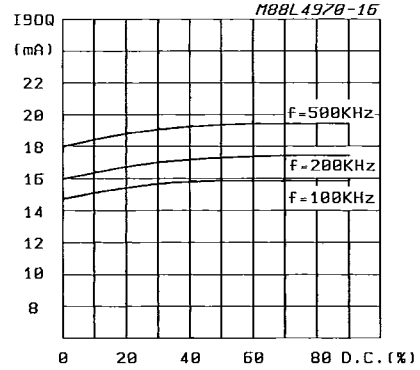


Figure 11 : Reference Voltage (pin 14) vs. V_i (see fig. 7).

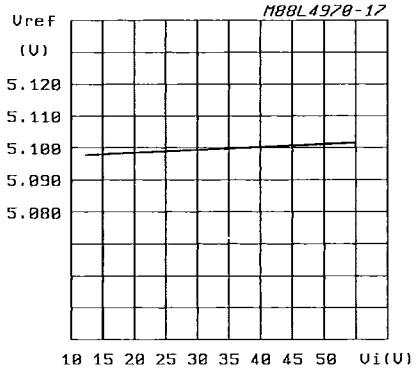


Figure 12 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

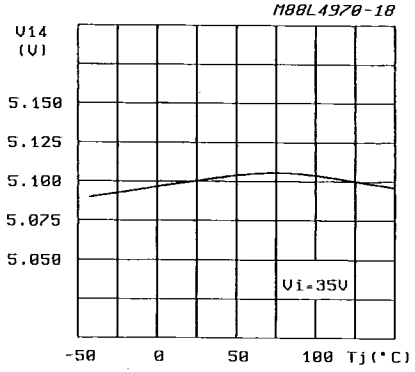


Figure 13 : Reference Voltage (pin 15) vs. V_i (see fig. 7).

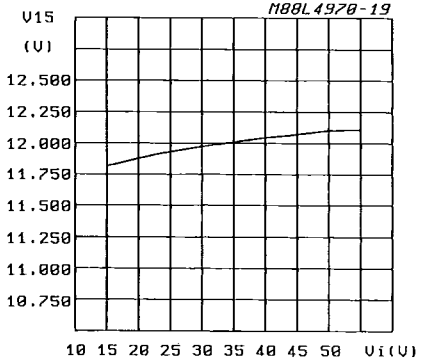


Figure 14 : Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7).

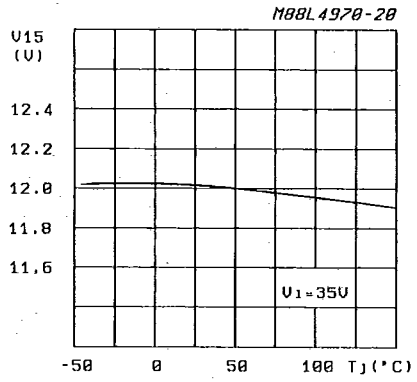


Figure 15 : Reference Voltage 5.1V (pin 14) Supply Voltage Ripple Rejection vs. Frequency.

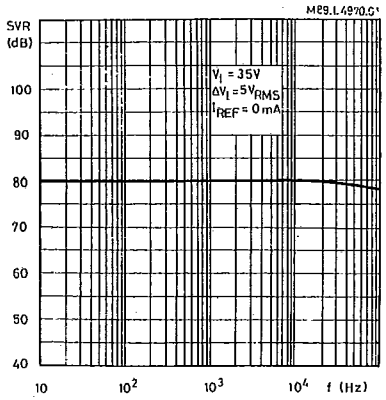


Figure 16 : Switching Frequency vs. Input Voltage (see fig.5).

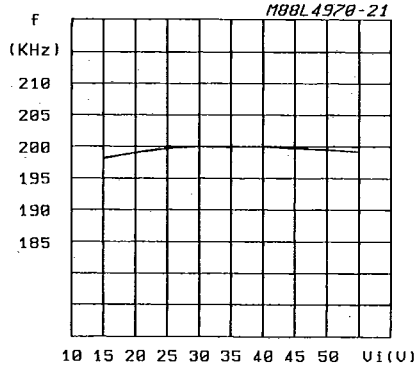


Figure 17 : Switching Frequency vs. Junction Temperature (see fig. 5).

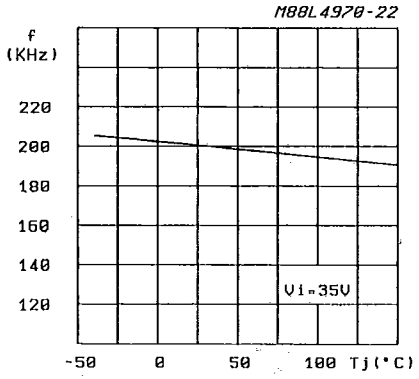


Figure 18 : Switching Frequency vs. R4 (see fig 5).

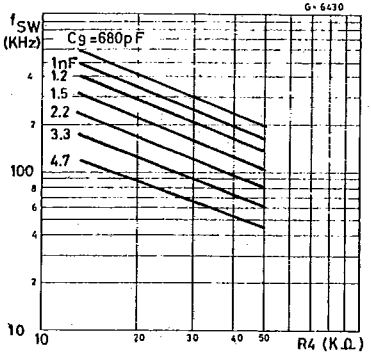


Figure 19 : Open Loop Frequency and Phase Response of Error Amplifier (see fig. 7C).

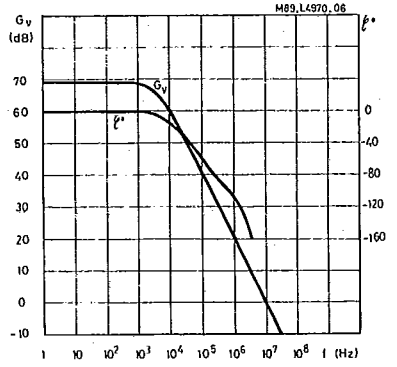


Figure 20 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 5).

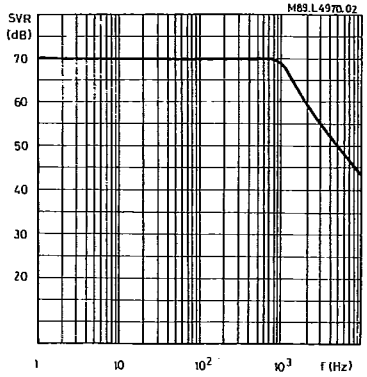


Figure 21 : Line Transient Response (see fig. 5).

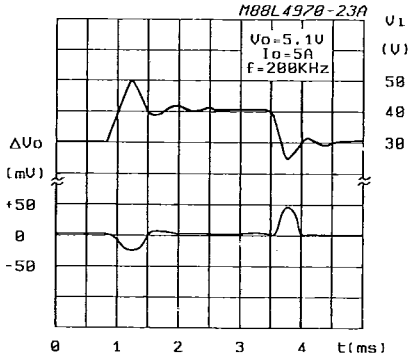


Figure 22 : Load Transient Response (see fig. 5).

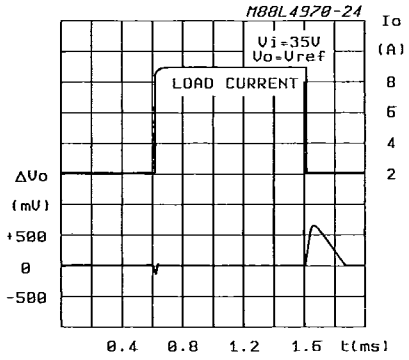


Figure 23 : Dropout Voltage between Pin 9 and Pin 7 vs. Current at Pin 7.

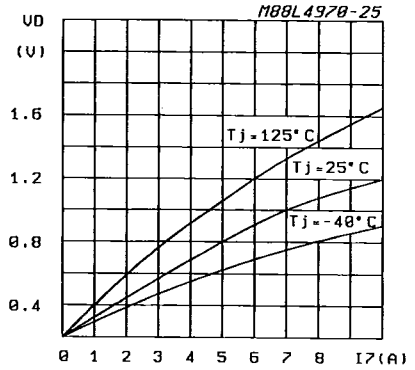


Figure 24 : Dropout Voltage between Pin 9 and Pin 7 vs. Junction Temperature.

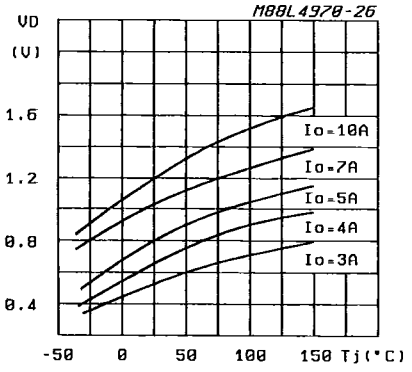


Figure 25 : Power Dissipation (device only) vs. Output Voltage.

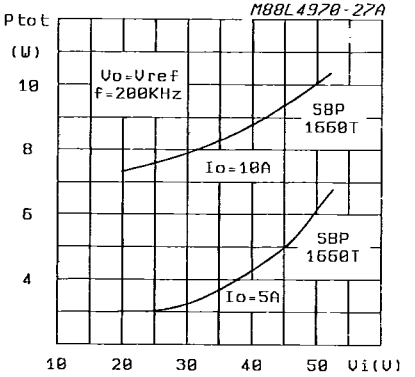


Figure 26 : Power Dissipation (device only) vs. Output Voltage.

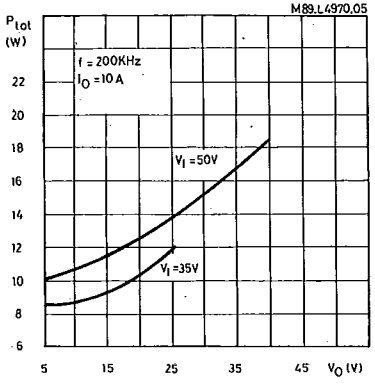


Figure 27 : Heatsink Used to Derive theDevice's Power Dissipation.

$$(R_{th-heatsink} = \frac{T_{case} - T_{amb}}{P_d})$$

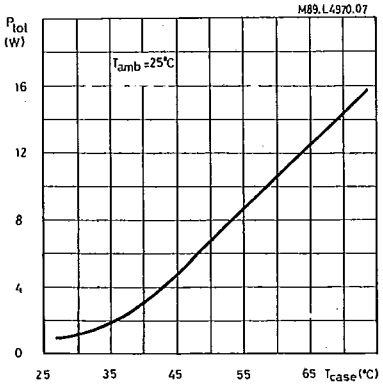


Figure 28 : Efficiency vs. Output Current.

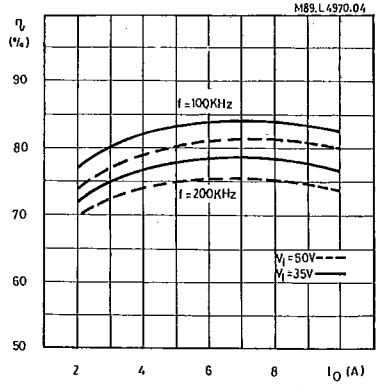


Figure 29 : Efficiency vs. Output Voltage.

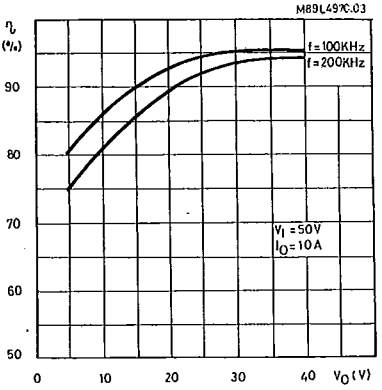


Figure 30 : Efficiency vs. Output Voltage.

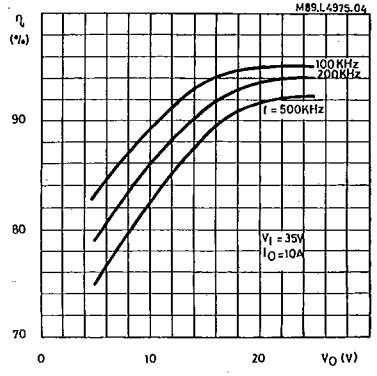


Figure 31 : Power Dissipation Derating Curve.

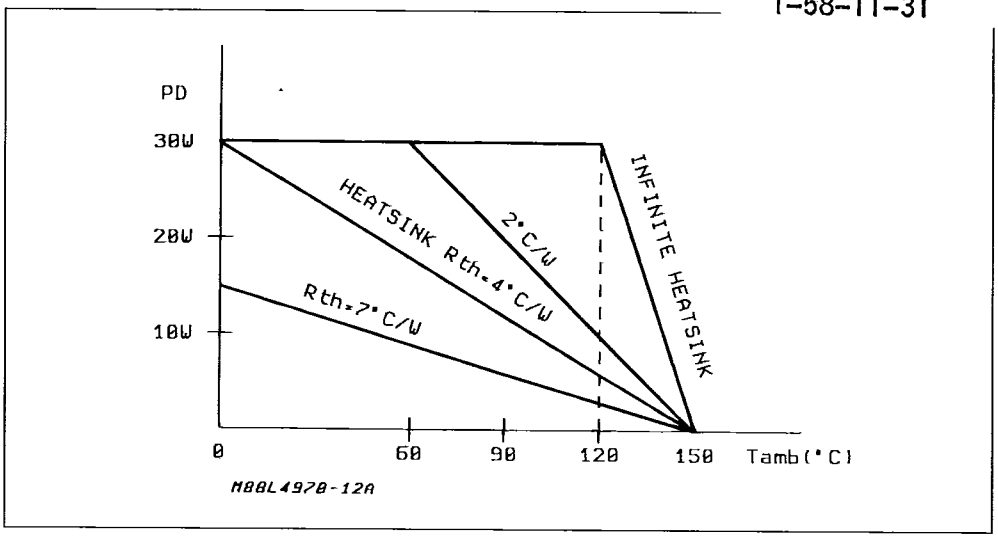
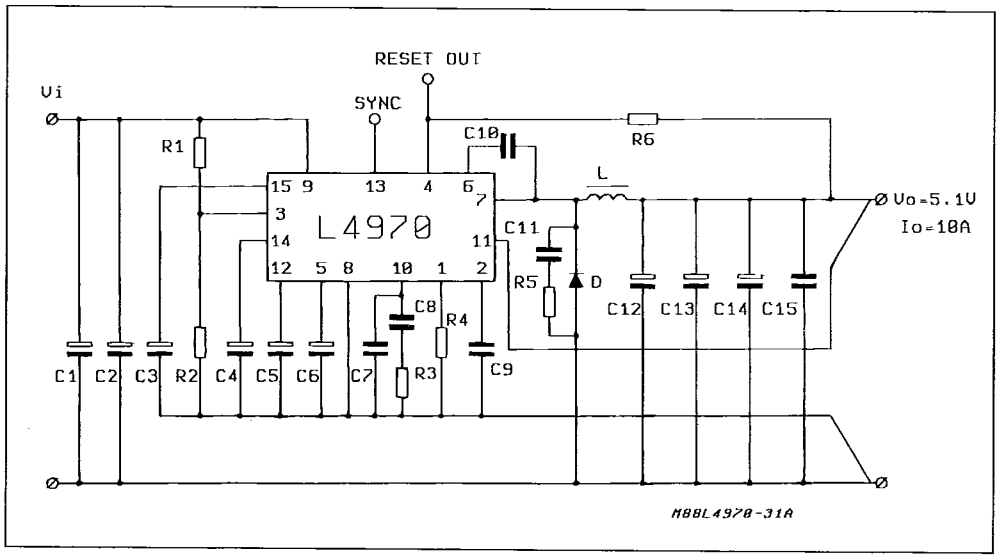


Figure 32 : 10A - 5.1V Application Circuit.



TYPICAL PERFORMANCES :

n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 10A ; f_{SW} = 200KHz)

$V_{o\ RIPPLE}$ = 30mV (at 10A)

Line regulation = 5mV (V_i = 15 to 50V)

Load regulation = 15mV (I_o = 2 to 10A)

For component values, refer to test circuit part list.

Figure 33 : 5.1V / 10A Low Cost Application (for component values refer to the test circuit part list).

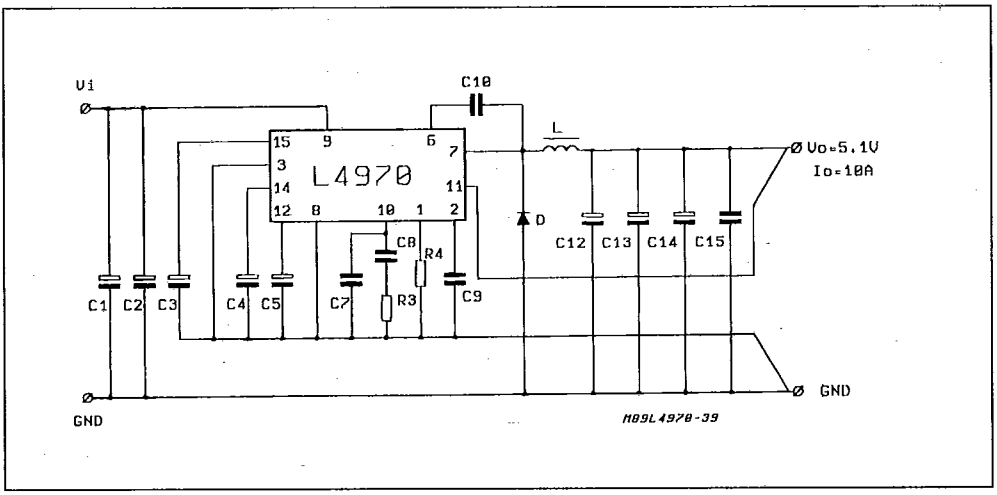


Figure 34 : 5.1V / 12V Multiple Supply. Note the Synchronization between the L4970 and the L4974.

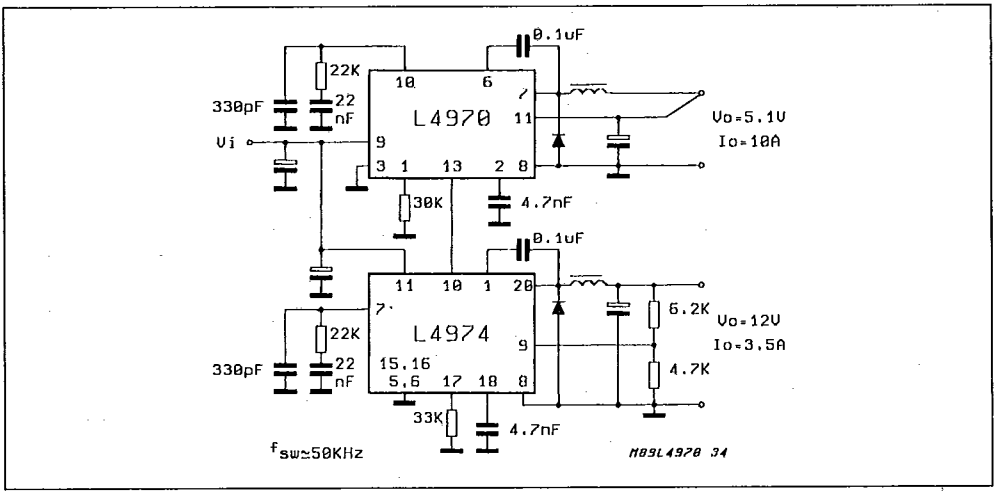


Figure 35 : L4970's Sync. Example.

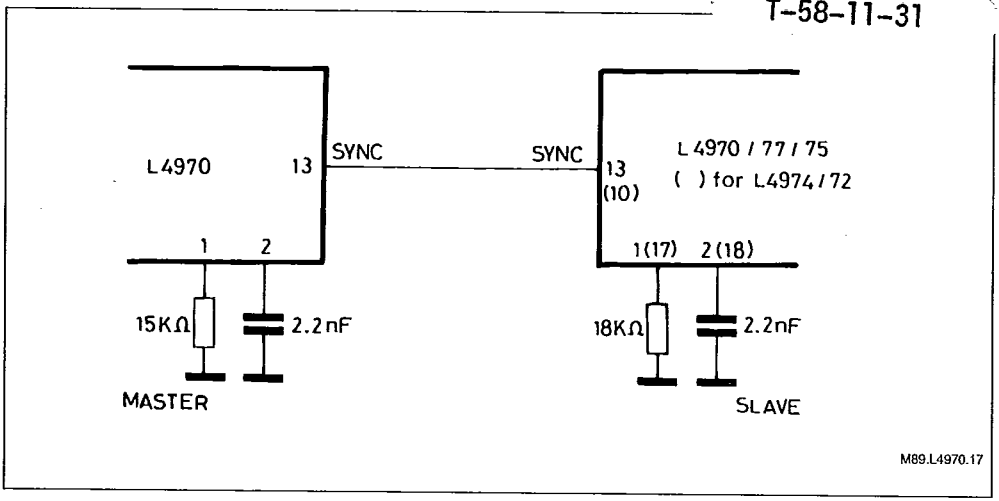


Figure 36 : 10A Switching Regulator, Adjustable from 0V to 25V.