Two Transistors Form Bidirectional Level Translator

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You often need to convert a logic signal from one power supply voltage to another. This conversion is a relatively simple task, unless the signal happens to be bi-directional. Serial buses such as Access.bus, I^2C, and SBI use bi-directional data lines. Some buses may require translating logic from one voltage to another; for example, from 3V to 5V. Figure 1 shows a simple solution to the conversion problem. The input signal can come from either side. In fact, you can drive both inputs low simultaneously (as in the I^2C bus) without incurring latchup.

This example illustrates a translation from 5V to 3V, but it can accommodate almost any other voltage levels, provided the logic-low levels are equal (usually 0V). translations from 1 to 10V are possible, albeit rather slow. The key to this circuit is the unusual cross-coupling of the emitters to the collectors. When you drive on input terminal low, the opposite transistor acts as a common base amplifier that saturates, pulling the other terminal low to within one Vcesat. This action also pulls the emitter of the input transistor low, to within one Vcesat of its collector, thereby cutting off collector current (although base current flows) and preventing latchup.

It is important that the base resistors R2 both connect to the lower voltage supply. Tests show that the circuit operates easily up to 300kHz. The major impediment to fast operation is the delay that occurs when Q1 comes out of saturation on a rising edge. The PSPICE simulation in Figure 2 shows the glitch this delay causes.

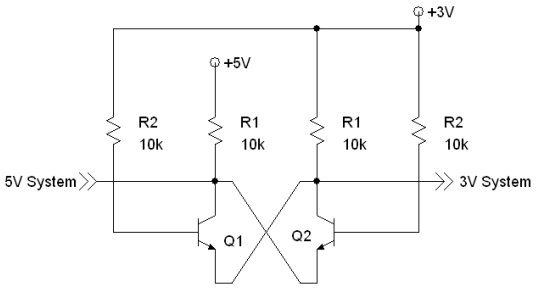

Figure 1. *Configured like two dogs swallowing each other's tails, this unusual two transistor configuration provides bi-directional logic-level shifting.*

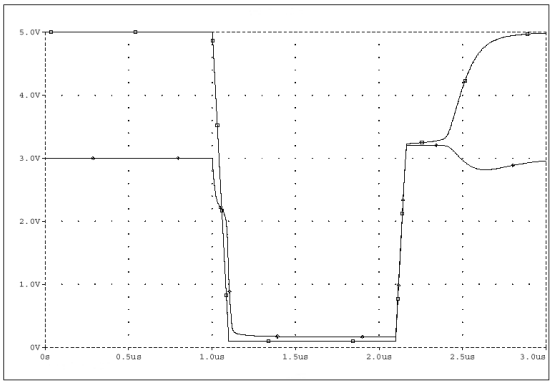

Figure 2*. A delay in exiting from hard saturation causes a glitch in the positive-going wavefront, thereby setting a limit on the speed performance of Figure 1's circuit.*