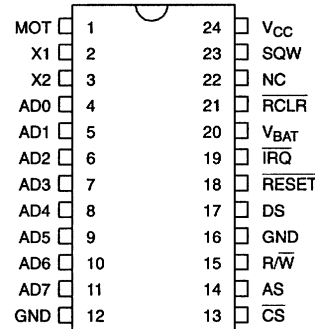


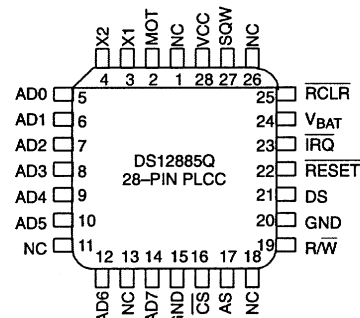
### FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin configuration closely matches MC146818B and DS1285
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation valid up to 2100
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
- 14 bytes of clock and control registers
- 114 bytes of general purpose RAM
- Programmable square wave output signal Bus compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable
- Time-of-day alarm once/second to once/day
- Periodic rates from 122  $\mu$ s to 500 ms
- End of clock update cycle
- Optional 28-pin PLCC surface mount package or 32-pin TQFP
- Optional industrial temperature range available

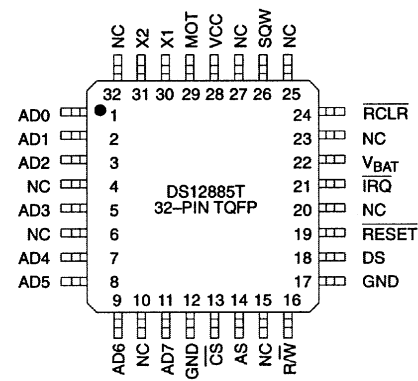
### PIN ASSIGNMENT



DS12885 24-PIN DIP  
 DS12885S 24-PIN SOIC



DS12885Q  
 28-PIN PLCC



DS12885T  
 32-PIN TQFP

## DESCRIPTION

The DS12885 Real Time Clock plus RAM is designed to be a direct replacement for the DS1285. The DS12885 is identical in form, fit, and function to the DS1285, and has an additional 64 bytes of general purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2,  $V_{BAT}$ , and  $\overline{RCLR}$ , see the DS12887 data sheet.

## PIN DESCRIPTION

|                    |                                |                   |  |
|--------------------|--------------------------------|-------------------|--|
| AD0–AD7            | – Multiplexed Address/Data Bus | $\overline{IRQ}$  | – Interrupt Request Output<br>(open drain) |
| NC                 | – No Connection                |                   |  |
| MOT                | – Bus Type Selection           | SQW               | – Square Wave Output                       |
| $\overline{CS}$    | – Chip Select                  | $V_{CC}$          | – +5V Supply                               |
| AS                 | – Address Strobe               | GND               | – Ground                                   |
| $R/\overline{W}$   | – Read/Write Input             | X1,X2             | – 32.768 kHz Crystal<br>Connections        |
| DS                 | – Data Strobe                  | $V_{BAT}$         | – +3V Battery Input                        |
| $\overline{RESET}$ | – Reset Input                  | $\overline{RCLR}$ | – RAM Clear                                |

## PIN DESCRIPTION

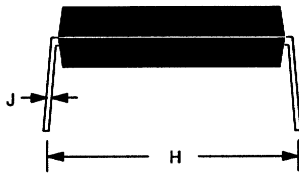
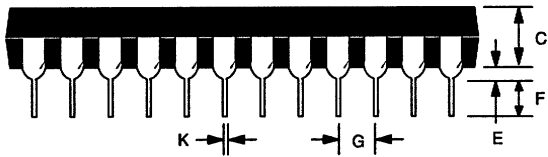
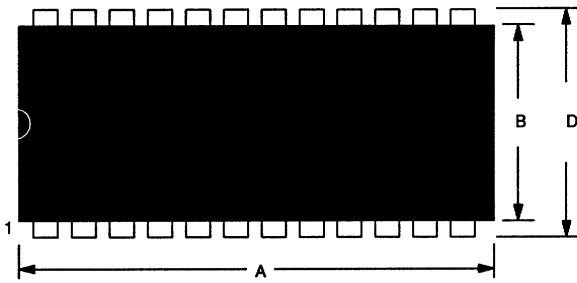
**X1, X2** – Connections for a standard 32.768 kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. The crystal is connected directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, “Crystal Considerations with Dallas Real Time Clocks.”

$V_{BAT}$  – Battery input for any standard 3-volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 4 volts for proper operation. A maximum load of 0.5  $\mu$ A at 25°C in the absence of power should be used to size the external energy source.

The battery should be connected directly to the  $V_{BAT}$  pin. A diode must not be placed in series with the battery to the  $V_{BAT}$  pin. Furthermore, a diode is not necessary because reverse charging current protection circuitry is provided internal to the device and has passed the requirements of Underwriters Laboratories for UL listing.

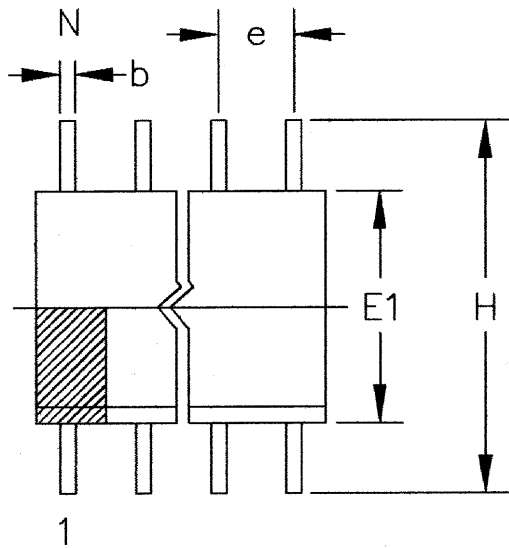
$\overline{RCLR}$  – The  $\overline{RCLR}$  pin is used to clear (set to logic 1) all 114 bytes of general purpose RAM but does not affect the RAM associated with the real time clock. In order to clear the RAM,  $\overline{RCLR}$  must be forced to an input logic “0” (–0.3 to +0.8 volts) during battery back-up mode when  $V_{CC}$  is not applied. The  $\overline{RCLR}$  function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. This pin is internally pulled up. Do not use an external pull-up resistor on this pin.

# DS12885 24-PIN DIP

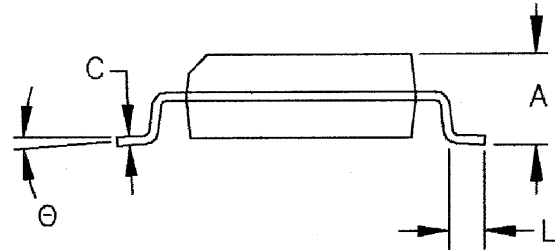
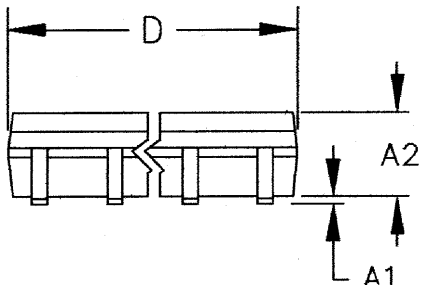


| PKG<br>DIM | 24-PIN |       |
|------------|--------|-------|
|            | MIN    | MAX   |
| A IN.      | 1.245  | 1.270 |
| MM         | 31.62  | 32.25 |
| B IN.      | 0.530  | 0.550 |
| MM         | 13.46  | 13.97 |
| C IN.      | 0.145  | 0.165 |
| MM         | 3.68   | 4.19  |
| D IN.      | 0.600  | 0.625 |
| MM         | 15.24  | 15.88 |
| E IN.      | 0.015  | 0.050 |
| MM         | 0.380  | 1.27  |
| F IN.      | 0.120  | 0.145 |
| MM         | 3.05   | 3.68  |
| G IN.      | 0.090  | 0.110 |
| MM         | 2.29   | 2.79  |
| H IN.      | 0.625  | 0.675 |
| MM         | 15.88  | 17.15 |
| J IN.      | 0.008  | 0.012 |
| MM         | 0.20   | 0.30  |
| K IN.      | 0.015  | 0.022 |
| MM         | 0.38   | 0.559 |

## DS12885 24-PIN SOIC



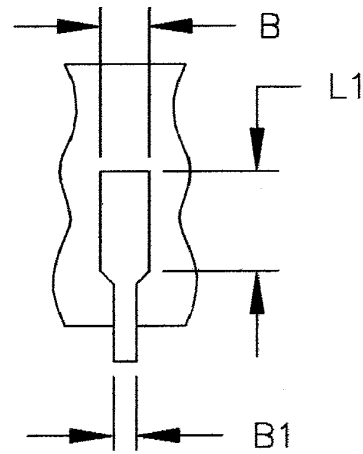
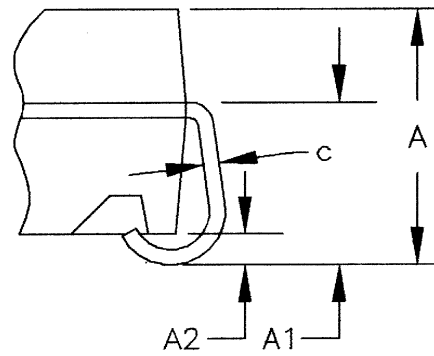
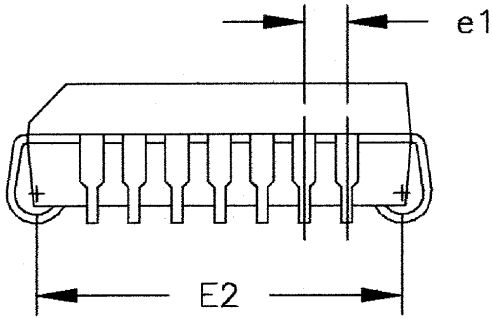
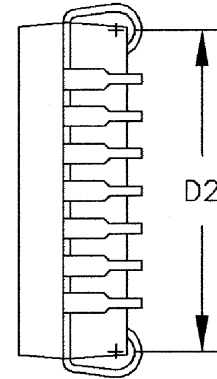
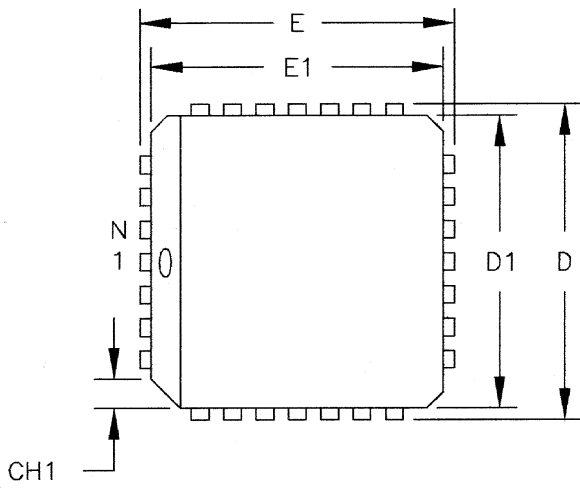
1



|    | LTR      | MIN   | MAX   |
|----|----------|-------|-------|
| A  | IN.      | 0.094 | 0.105 |
|    | MM       | 2.39  | 2.67  |
| A1 | IN       | 0.004 | 0.012 |
|    | MM       | 0.102 | 0.30  |
| A2 | IN       | 0.089 | 0.095 |
|    | MM       | 2.26  | 2.41  |
| B  | IN       | 0.013 | 0.020 |
|    | MM       | 0.33  | 0.51  |
| C  | IN       | 0.009 | 0.013 |
|    | MM       | 0.229 | 0.33  |
| D  | IN       | 0.598 | 0.612 |
|    | MM       | 15.19 | 15.54 |
| E  | IN       | .050  | BSC   |
|    | MM       | 1.27  | BSC   |
| E1 | IN       | 0.290 | 0.300 |
|    | MM       | 7.37  | 7.62  |
| H  | IN       | 0.398 | 0.416 |
|    | MM       | 10.11 | 10.57 |
| L  | IN       | 0.016 | 0.040 |
|    | MM       | 0.40  | 1.02  |
|    | $\theta$ | 0°    | 8°    |

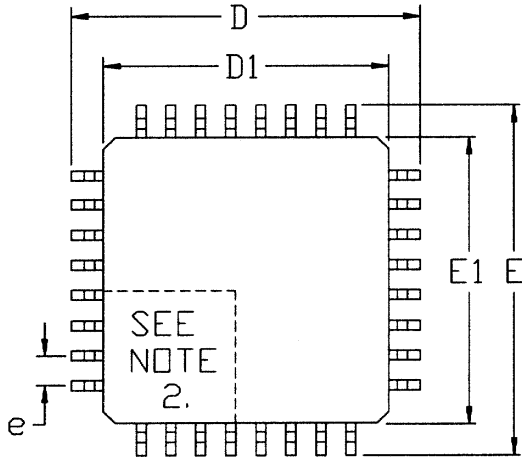
The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that  $\frac{1}{2}$  or more of it's area is contained in the hatched zone.

**DS12885Q 28-PIN PLCC**

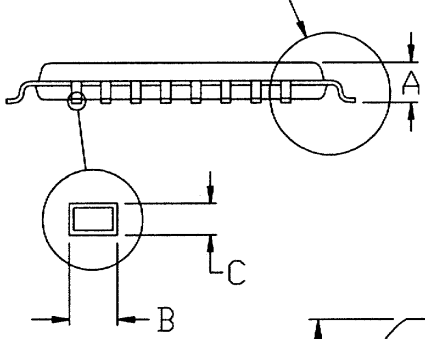


| LTR | MIN      | MAX  |
|-----|----------|------|
| A   | .165     | .180 |
| A1  | .090     | .120 |
| A2  | .020     | -    |
| B   | 0.26     | .033 |
| B1  | .013     | .021 |
| C   | .009     | .012 |
| D   | .485     | .495 |
| D1  | .450     | .456 |
| D2  | .390     | .430 |
| E   | .485     | .495 |
| E1  | .450     | .456 |
| E2  | .390     | .430 |
| L1  | .060     | -    |
| N   | 28       | -    |
| E1  | .050 BSC |      |
| CH1 | .042     | .048 |

**DS12885T 32-PIN TQFP**



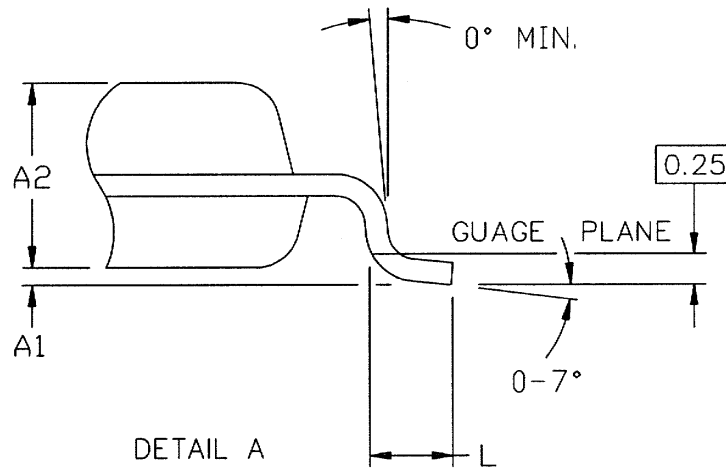
SEE DETAIL "A"



| DIM | MIN  | MAX  |
|-----|------|------|
| A   | -    | 1.20 |
| A1  | 0.05 | 0.15 |
| A2  | 0.95 | 1.05 |
| D   | 8.80 | 9.20 |
| D1  | 7.00 | BSC  |
| E   | 8.80 | 9.20 |
| E1  | 7.00 | BSC  |
| L   | 0.45 | 0.75 |
| e   | 0.80 | BSC  |
| B   | 0.30 | 0.45 |
| C   | 0.09 | 0.20 |

NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; AT MAXIMUM MATERIAL CONDITION. PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.
4. CONTROLLING DIMENSIONS: MILLIMETERS.



DIMENSIONS ARE IN MILLIMETERS