Differential VCO for PMR446 system

Juha S. Hallivuori and Petri J. Korpi

***Abstract*—A differential negative-Gm LC oscillator was designed to PMR446 system. An IC type of VCO configuration was used for to find out if it would be suitable also for a discrete component VCO. A 4–MHz frequency control range was achieved over the wanted frequency band and phase noise of -89 dBc/Hz at 12.5-kHz offset frequency. Output power of +11 dBm was reached with 62 mA of current consumption from 5 V supply.**

***Index Terms*—differential, LC oscillator, VCO**

I. Introduction

THE interest in PMR446 system design and implementation of an RF VCO with discrete components using a topology from IC world [1] were the key motivators for this project. The RF VCO provides the local oscillator signal for the first down conversion mixer in the receiver RF chain. The RF VCO was identified by the authors to be one of the hardest blocks to design because of the very tight phase noise specification and high output power. Probably the best topologies to implement this kind of very low phase noise VCO are to use the old Colpits or Hartley type oscillator topologies with passive impedance matching circuit at the output. We did not want to do that because those are already tested and known to be suitable for discrete VCO designs. We wanted to try how a differential VCO topology with active buffer at the output would perform in PMR446 system. One interesting point to see was how the two differential paths of the VCO would look like because the PCB board and discrete components cannot be exactly differential; another point was the discrete component high device-to-device value variation effects.

The key specifications of the VCO are shown in Table I. The current consumption specification was relieved from total current of 20 mA to core current of 20 mA after initial discussions. With 20 mA current for the VCO core and the 42 mA current for the output buffer we get over +10 dBm output power.

This paper introduces a differential negative-Gm based voltage controlled oscillator, which operates in the frequency band from 421.3 MHz to 425.3 MHz and has PN junction varactor frequency control and emitter follower output buffer. In the II part, the VCO topology is presented and the design and simulation of the circuit are explained. In part III, the measurement setup and measurement results are presented and some differences between simulation and measurement results are discussed. Finally, in part IV, conclusions are drawn.

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II. Design

In the reference [2] thorough description of the LC oscillator theory is presented. The design started with a calculation of the resonance frequency with the equation (1).

$$\omega_1 = \sqrt{\frac{L_P}{C_P}} \qquad (1)$$

where L_P is the parallel resonator tank inductance and C_P is the parallel resonator tank capacitance. Figure 1 shows an illustration of a parallel resonance circuit. There a series parasitic resistance R_S of the tank inductance is converted to an equivalent parallel resistance component R_P. One can see that when at resonance, according to equation (2), the inductive and capacitive parts cancel each other out and only remaining component is R_p. This can be clarified with Figure 1.

$$jL_P\omega = \frac{1}{jC_P\omega} \qquad (2)$$

This remaining loss component of the tank is then cancelled with negative R produced with positive feedback. That is used to define the transistor g_m according to equation for the core small signal gain $G = -g_{m1}R_P$ which equals to 1.

TABLE I
KEY SPECIFICATIONS.

	Specification
Fosc, min	424.0 MHz
Fosc, max	425.3 MHz
Pout	10 dBm
Phnoise 12.5 kHz	-117 dBc/Hz
Phnoise 1 MHz	-157 dBc/Hz
Output power variation	2 dB
Frequency control sensitivity	Max 0.5 MHz/V
VCO core current consumption	Max 20 mA

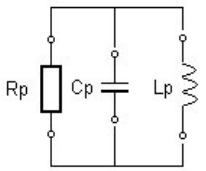

Fig 1. Resonance tank with parallel components.

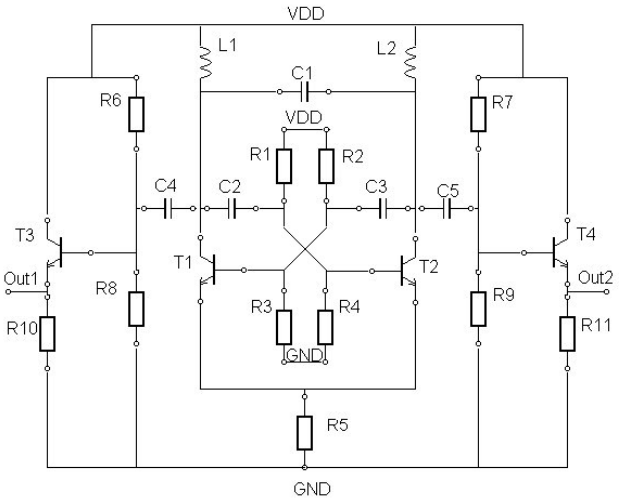

Fig. 2. Bipolar LC-VCO schematic with emitter follower buffer. Some emitter and collector bias resistors were added after some failures in dc bias point setting.

VCO design cycle was as follows: The choice of a suitable transistor, preliminary simulations, PCB design, preliminary measurements, problem solving and corrections for the next version.

A typical bipolar VCO schematic is shown in Figure 2. This structure is widely used in integrated circuits and we decided to test the suitability of this structure in a PCB-scale implementation. At first, the Agilent ADS was used to determine different component values, and the core transistors. A commonly used bipolar transistor BFG520 was chosen. According to the simulations the specified targets should be achieved with this transistor. But as it turned out the VCO did not even oscillate with the simulated component values and the whole project became more or less just component soldering exercise.

The first build and measured board did not work at all because the inductor that was used had too low Q value and because the cross connection in the transistor bases were done with a jump wires that where quite lossy.

The next two versions also suffered from the same problem of low inductor Q. Furthermore the buffer oscillated on its own because of bad groundings. In the fourth and the fifth board, we improved the grounding and resorted to higher inductor Q's in all boards constructed so far. Finally we got the first board, with PHEMT (ATF-35143) high power transistors to oscillate.

As the oscillation commenced after the changes also in other trial boards we decided that the bipolar transistor should be used. This was due to its lower cost.

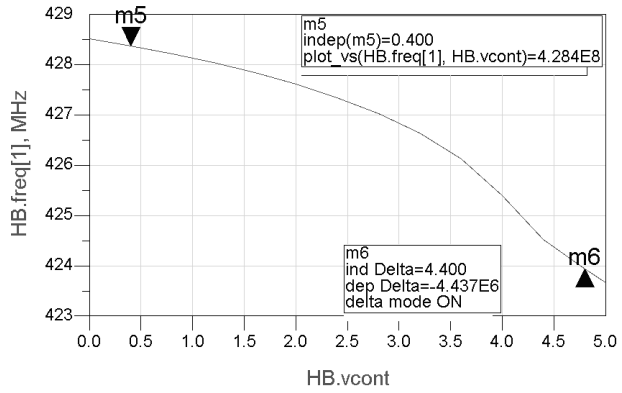

Fig. 3. Simulated frequency tuning curve of the VCO, simulation fulfils the specification with good enough margin.

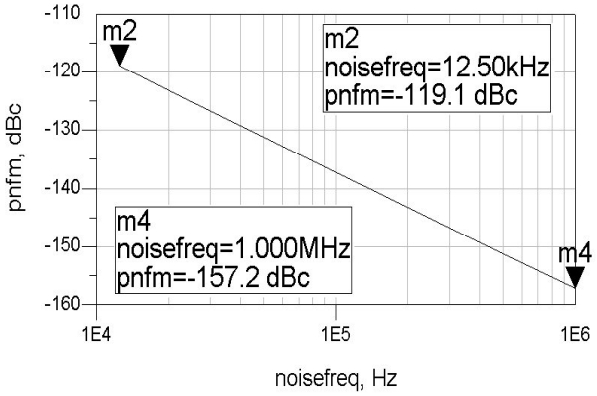

Fig. 4. Simulated phase noise of the VCO, simulation fulfils the specification with some margin.

The simulated frequency-tuning curve is shown in Figure 3. The adequate frequency range was achieved easily. The simulated frequency curve is a bit too steep but usually the curve observed is more flat in actual measurements than is simulations. This is because of the parasitic capacitances that arise from the PCB and from discrete components that are connected parallel with the varactor connected bipolar transistors. And thus the tuning range is reduced because the fixed capacitance value is increased while the tunable capacitor remains the same. The simulated phase noise curve of the VCO is presented in Figure 4. The simulated phase noise values fulfill the specification values with some margin.

The layout of the final VCO PCB board is shown in Figure 5. The main transistors are cross-coupled in the middle of the board, buffer transistors are located at both sides and the varactor connected bipolar transistors are above the cross-coupled pair. The resonance circuit is in the middle of the board below the varactor connected bipolar transistors.

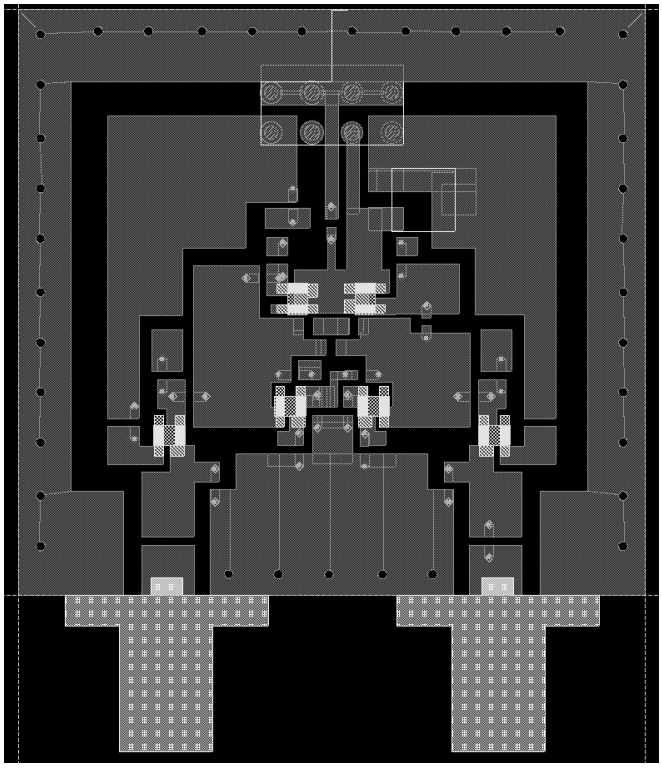

Fig. 5. Layout for the VCO, due to the differential structure the actives at the left side have to be flipped.

III. TEST RESULTS

The final LC-VCO was measured against the specifications. For VCO's there are many test setups and measurement systems available on the market. The VCO-PLL measurement system HP4352B VCO/PLL Signal Analyzer from Hewlett-Packard was used in this work. This equipment is solely for VCO measurements and is highly automated. It has low noise power and control supplies for the DUT. The phase noise (PN) measurement accuracy at 12.5 kHz offset is -134 dBc/Hz which was enough for this work.

Due to the high DC power needed for the VCO the current supply was fed from a stand-alone supply. This did not effect on phase noise results and, because the pushing figure was not required, it did not complicate the needed measurement either. Required measurements: phase noise measurement at 12.5 kHz and 1 MHz offsets, tuning range and the tuning gain. Current consumption specification was defined at early stage to contain only the core current; this was due to the selected structure and the high output power needed.

So in the measurement two similar VCOs were measured and compared with simulated values as well as with the specifications. The measurements were carried out using HP4352B VCO/PLL Signal Analyzer with HP43521A down converter unit and HP8665B Synthesized Signal Generator, and Thurlby/Thander PL310QMD voltage source. An external balun (Minicircuits ZFSCJ-2-4) was used to combine the power from the differential output signals.

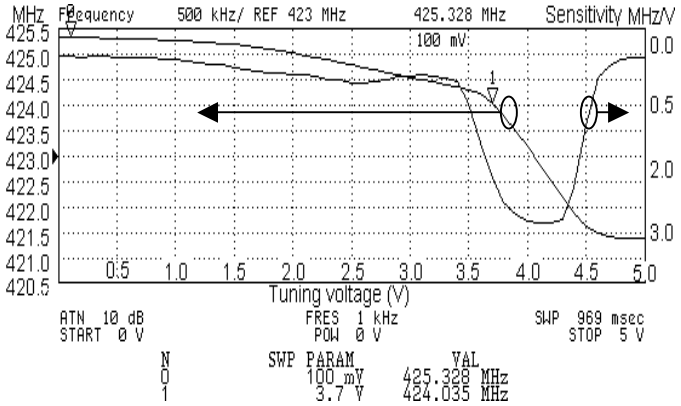

Fig. 6. Measured frequency and sensitivity curve of the VCO vs. control voltage.

One problem in the measurements was also to get the oscillation frequency right on the middle of the wanted frequency band because the frequency range was only 1.3 MHz. The oscillation frequency drifted because the VCO was free running and not inside a PLL loop. Also the values of the discrete components varied so much that the search of the right oscillation frequency required a lot of tuning.

As anticipated from the prior knowledge and first trials the simulations of the VCO were noticed to be inaccurate. So the main target at first was just to get the prototype to work in the measurements. After that, the measurement revealed that the noise models in the transistor were not suitable for the VCO design because the real noise performance was 30 dBs worse than the simulated value. Other measured results, however are closer to simulated values. Figure 6 shows the measured oscillation frequency over the tuning voltage and tuning sensitivity of the VCO. The sensitivity is below the 0.5 MHz/V value up to 3.7 V control voltage value where the adequate frequency control range of 1.3 MHz is reached. The tuning range has to be bigger than specified, because of the component variations and the actual available size of the components.

It is not possible to achieve exactly the same oscillation frequency in two units. Depending on component tolerances the actual tuning range might need to be some 3 times the tuning range needed in operation. And actually if real manufacturing aspects are to be considered some 5 to 10 times specified tuning range should be designed. This VCO achieves the tuning range needed in operation with correct tuning gain, but has some problems achieving lower end frequency specified.

Phase noise measurement can be seen in Figure 7, the plateau area is mainly from the buffer noise floor and the 20 dB/dec area is from the core. The results fail to fulfill the specifications and the main reason seems to lie in the differential pair. Even though the resonance circuit is only with modest Q value, testing with other, more expensive active components gains at least 10 dB improvement in phase noise at 12.5 kHz offset.

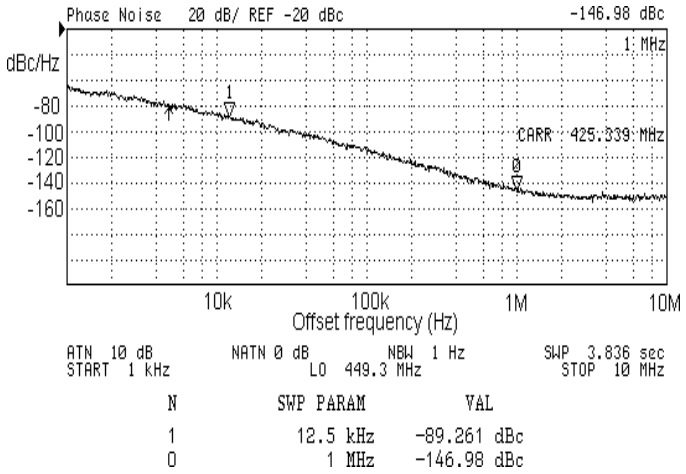

Fig. 7. Measured phase noise of the VCO vs. offset frequency.

TABLE II
SPECIFICATIONS, SIMULATED AND MEASURED RESULTS.

	Specification	Simulations	Measurements
Fosc, min	424.0 MHz	419.0 MHz	421 MHz
Fosc, max	425.3 MHz	427 MHz	425.3 MHz
Pout	10 dBm	11 dBm	11 dBm
Phnoise 12.5 kHz	-117 dBc/Hz	-119.1 dBc/Hz	-89.2 dBc/Hz
Phnoise 1 MHz	-157 dBc/Hz	-157.2 dBc/Hz	-147 dBc/Hz
Output power variation	2 dB	0.05 dB	0.1 dB
Frequency control sensitivity	Max 0.5 MHz/V	0.5 MHz/V	0.5 MHz/V
VCO core current	20 mA	20 mA	20 mA

Comparison to the simulated results reveals major problems on noise modeling in the bipolar transistors and resonance Q. See Figures 4 and 7.

During the design phase a simulator was used to try to improve the VCO PN. However each trial, which improved the PN in simulations, failed to do so in measurements. Probably some -105 dBc/Hz at 12.5 kHz would be achievable with better transistors. This claim is based on the PHEMT (ATF-35143) VCO measurements. Naturally, the change of transistors would have resulted in a 10 times more expensive design. Output power and the tuning specifications are achievable, however.

The balance between the two differential VCO outputs was found to be quite good. The suppression of the second harmonic was some 30dB's when the output was changed from single-ended to differential signal. Specifications, simulation values and measured frequency range, output power, phase noise and control voltage sensitivity are summarized to Table II.

IV. CONCLUSIONS

As noticed from the results the most important specification the phase noise specification is not fulfilled diminishing the quality of the VCO. However, the PN specification was proven to be very difficult to meet and probably achievable only with a phase locked loop (PLL) with crystal oscillator. The PLL is also needed to control the VCO slow frequency drift, which is in here higher than the channel frequency band. The output power and frequency range specifications were met and the selected topology was proven to work in PCB as discrete realization. To manage with the specifications one should test and measure other transistor choises, to be able to really optimize the phase noise.

ACKNOWLEDGMENTS

The authors thank Nokia Research Center for providing simulation and measurement tools and equipment. A special thank to Panu Siukonen for sending the external balun for the output power combining.

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