5 Technical Description

5.1 Automatic Start-up Sequence (X-Band)

The automatic start-up sequence described below, should be read in conjunction with Figures 1.30 'X-Band Turning Unit (Aloft) Schematic'.

5.1.1 Start-up

Important Notice *- Once mains is applied to the PSU board the Power Factor Correction (PFC) circuitry starts and generates 390V. It should be noted that whilst mains is applied the PFC is active and cannot be manually switched off. The start circuitry only controls the flyback converter so High Voltage DC is present on primary power components whenever mains is present on the board.* ***This fact should be noted when servicing the Transceiver.***

The Power Supply in the Transceiver is only active during normal operation when there is a Display (or Compatibility Unit) connected to it. The RS422 serial data stream from the Display is used to drive an opto-coupler in the PSU which detects the presence of either polarity voltage and enables the flyback converter in the PSU.

The RS422 serial data stream from the Display enters the Input Board on connector TSB 1, 2 as "DU DATA+ and DU DATA-". It is then passed to the Trigger Board via PLYB 16, 17, and then on to the PSU via PLTH 11, 12 (as PSU START and PSU START RTN).

For test purposes the PSU can be turned on in the absence of a serial data stream by linking pins 1-2 on LKA (PSU).

5.1.2 Transmit Enable

When the operator selects Transmit, the TU Enable signal is activated LOW on the Trigger PCB (PLYH 10). On the X-Band Scanner Unit, this signal is fed to the Power Supply Unit and via the Turning Unit On/Off and Input PCB to the Motor Drive PCB to start the antenna rotating.

Once the antenna has done one complete revolution transmission is started. When standby is selected, transmission is immediately halted and, after one complete revolution of the antenna, TU Enable is disabled.

The Modulator starts to generate radar pulses when the Trigger PCB sends it MOD TRIGGER pulses (to PLVC 9). Note that the CHARGE TRIGGER pulses (on PLVC 8) are present even in Standby mode.

A signal indicating that the Magnetron has fired is fed via MAG SAMPLE from PLVC 7 on the Modulator PCB to the Trigger PCB. This signal is processed on the Trigger PCB and outputted as TX TRIG (PLYB 20 & 21) to the Input PCB (PLZB 20 & 21) and then to the Display Unit via TSB 5 & 6.

Note *- TX DATA is sent from the Transceiver to the Display Unit.*
DU DATA is sent from the Display Unit to the Transceiver Unit.

The Trigger PCB processes the serial data input from the display, and generates the required control signals for the Transceiver.The data is transmitted each time a bearing pulse is received from the Turning Unit. The various timing signals required by the Transceiver including the Pulse Repetition Frequency (PRF), are generated by the Trigger pcb.

5.1.3 Transmitter Operation

The high-voltage negative pulses required to drive the magnetron are generated by the Modulator PCB.The modulator pulse widths are selected by the Trigger pcb but are defined by the Modulator pcb.Timing signals are controlled from the Trigger pcb. A spark gap on the Modulator is fired if the magnetron fails to operate. Continual operation of the spark gap is detected and a signal is fed back to the Trigger pcb, as the spark gap detect signal.

When the spark gap detect signal reaches approximately 2.5v, the microcontroller inhibits transmission for approximately one second. On detection of this signal, the Trigger pcb switches the radar to Standby, and generates an error signal which is transmitted to the Display Unit via the serial data link.

When Standby is selected, rotation of the Antenna is inhibited. Unless in Test Mode, transmission from the radar is inhibited if the Antenna is not rotating.

On the Trigger PCB, there is a timer circuit which is basically a capacitor that slowly discharges (between 4s and 18s) when power is removed from the PCB. On power-up the microcontroller measures the charge remaining on the capacitor to determine whether the transceiver has been switched off for long enough to warrant inhibiting transmit for three minutes until the magnetron heaters have had time to warm up again.

The other analogue signals into the Trigger PCB come from the Modulator. The Modulator supply voltage and the magnetron current (only when transmitting) are measured and sent to the Display as an aid to fault finding.

5.2 Trigger PCB (X Band)

5.2.1 General Description

The Trigger PCB controls the operation of the Transceiver under instruction from the Display. There are two serial links, which are used to transfer control messages from the Display to the Trigger PCB and Transceiver information back to the Display. The Trigger PCB generates control and tuning signals required by the Modulator, Receiver, Performance Monitor and Biased Limiter. The PSU is enabled with a signal from the Trigger PCB.

5.2.2 Signals To /From the Trigger PCB

To/From Display

Serial Data to Display
Serial Data from Display
Trigger to Display

To/From Modulator

Pulse Length select lines
Charge and Modulator Triggers
Magnetron Heater Turndown signal (only used for S-Band, Long Pulse operation)
Voltage/Current Monitor signals
10/25kW and X-Band Configuration signals

To/From Receiver

Tuning Voltage signal
Bandwidth Control signal
AFC/Manual control
AFC Trigger
Tune Indicator signal

To Biased Limiter

Trigger signal

To Performance Monitor

On/Off signal
Mode Control signal
Tuning Voltage signals

To/From Power Supply PCB

+30V, +12V, +5V, 0V & -12V Supply lines
Turning Unit Enable
Power Supply Start and Return

5.2.3 Functional Description (X-Band Trigger PCB)

The 80C51 family microcontroller provides overall control of the Trigger PCB functions. Program memory and RAM are included within the microcontroller IC. Serial I/O is handled by the microcontrollers internal UART and an external RS422A driver and receiver. Baud rate is fixed at 76800 baud for operational use but is link selectable to 19200 or 38400 baud for test purposes. The serial data format is 8-bit data, 1 stop bit and even parity.

The Display sends serial messages comprising four or five characters depending on message content. Control messages are four bytes long and tuning messages are five. The tuning voltage levels are sent as 12-bit values which are converted on the Trigger PCB using a four-channel DAC before amplification/buffering and distribution to the Receiver and Performance Monitor.

The Bearing signal from the Turning Unit is used to initiate serial transmission from the Trigger PCB such that each time one of the 4096 azimuth pulses per rev is generated and fed into one of the microcontrollers interrupt pins, a character (one byte) is sent to the Display. One bit in each of the characters sent is dedicated to the heading marker, on every new heading marker pulse from the Turning Unit, the bit is toggled.

The Power Supply in the Transceiver is only active during normal operation when there is a Display (or Compatibility Unit) connected to it. The RS422 serial input from the Display is used to drive an opto-isolator which detects the presence of either polarity voltage and enables the PSU.

Trigger Ouputs

There are a number of trigger signals generated by the Trigger PCB:

Pre-Trigger (optional)
Charge Trigger
Modulator Trigger
Display Trigger
Performance Monitor Trigger
AFC Trigger
Swept Attenuation Initiate

The Charge Trigger is the timing signal used to recharge the Modulator PFN. This is generated by the microcontroller using an internal timer routine set to the appropriate PRF for the pulse length selected. A wobbulation factor is added to the basic timing to ensure that no two radar transmissions are locked together. The wobbulation is calculated according to the number of serial messages received before going to transmit and the position of the antenna between each trigger pulse.

An optional Pre-trigger will be produced approximately 11μs before the modulator trigger. This is not a normally fitted option and is intended for use in special options applications.

The Modulator Trigger is used to discharge out the PFN into the magnetron and is the trigger that initiates the modulator firing. The PFN is recharged by the Charge Trigger pulse which follows100μs after each Modulator Trigger pulse. In standby mode, the Charge Trigger pulse is still generated, but the Modulator Trigger pulse is gated off.

In standby, the Display and Performance Monitor Triggers are generated from the Mod Trigger pulse. When the transceiver is in transmit mode the triggers begin on the leading edge of the magnetron sample pulse and end after a preset time, adjustable using RV1.

The AFC Trigger is used by the receiver when in AFC mode and is only generated when the transceiver is in transmit mode. The pulse is started on the front edge of the Modulator Trigger and terminates on the back edge of the magnetron sample pulse.

The Swept Attenuation Initiate pulse is the timing signal fed to the Limiter Drive PCB which generates the control for the biased limiter. It is initiated by the front edge of the Pre-trigger (approximately 2μs prior to magnetron firing) and terminated 2.5μs after the leading edge of the magnetron sample pulse.

The Display and PM Triggers are essentially the same trigger and are present at all times when the radar is powered up. They are initiated by the Modulator Pulse and last for approximately 2.5μs.

Analogue Outputs

The Trigger PCB generates four variable DC signals; LO.Tune, PM Tune, Xr Adjust and Xt Adjust. These signals are coded as 12-bit digital values and incorporated into the serial messages from the Display. A 12-bit, four channel DAC is used to generate the tuning signals from the message data. Additional buffering is added to the LO and PM Tune outputs of the DAC and x3.5 amplification to the Xr and Xt Adjust signals.

LO Tune is the 0V to +5V receiver tuning signal and PM Tune the 0V to +5V Performance Monitor main tuning signal. Xr and Xt Adjust are 0V to +15V signals used to control the receive and transmit attenuators in the Performance Monitor.

Analogue Inputs

There are various analogue inputs to the Trigger PCB from other PCBs in the transceiver and some on-board signals that are fed into an eight channel 8-bit ADC, and converted to digital values either for further processing by the microcontroller or to be passed to the Display via the serial message link.

The signals on the Trigger PCB that are measured are the dropout timer and +12V and +30V supplies. The timer circuit is basically a capacitor that slowly discharges (between 4s and 18s) when power is removed from the PCB. On power-up the microcontroller measures the charge remaining on the capacitor to determine whether the transceiver has been switched off for long enough to warrant inhibiting transmit for three minutes until the magnetron heaters have had time to warm up again. The power supply levels are measured and the results sent to the Display as an aid to fault diagnosis.

One channel of the ADC is used to detect whether a Performance Monitor has been fitted to the system. The voltage on this channel will be lower than a preset value if a Performance Monitor is present otherwise it will be pulled to the +5V supply rail. This information is encoded and sent as part of the configuration message to the Display.
The Receiver sends a tune indicator signal to the Trigger PCB which indicates how close it is to being on tune. This signal is coded as part of the serial message and sent to the Display.

The other analogue signals into the Trigger PCB come from the Modulator. The Modulator supply voltage and the magnetron current (only when transmitting) are measured and sent to the Display as an aid to fault finding. The spark gap detect signal is generated by the modulator when the spark gap arcs over, if it reaches a predetermined level the microcontroller inhibits transmission for approximately one second and sends an error message to the Display.

Digital Outputs

The digital outputs from the Trigger PCB are all straight forward on/off control signals to various parts of the transceiver.

Signals to the Receiver select wide or narrow bandwidth (Wideband) and AFC or manual tuning mode (AFC On). Narrowband is selected when the modulator is transmitting in long pulse and briefly during pulse length changing. AFC or manual mode is selected by the radar operator and is part of the control message sent from the Display.

Modulator signals MP and SP are used to set the pulse length as requested by the radar operator, SP set to 0V indicates short pulse operation, MP set to 0V indicates medium pulse operation and both SP and MP set to +5V indicates long pulse operation. SP and MP both set to 0V is an illegal state and will not happen in normal operation. Turndown enable is used to reduce the heater current in the magnetron and is only set when an S-Band magnetron is fitted and is transmitting in long pulse.

The control signals PM On/Off and PM Tx/Rx are used to switch the Performance Monitor on and to switch it between system test mode and receiver test mode.

TU Enable is the control signal fed to the Motor Drive PCB to initiate rotation of the antenna. When the operator selects transmit the TU Enable signal is activated to start the antenna rotating.

Once the antenna has done one complete revolution transmission is started. When standby is selected, transmission is immediately halted and, after one complete revolution of the antenna, TU Enable is disabled.

Optional I/O

There are several optional I/O signals for use with special options variants of the PCB; Pre-trigger (as described in the section on triggers), External Trigger Input and Radar Silence. The External Trigger input is used when the modulator needs to be triggered from an external source rather than the Trigger PCB. Trigger signals fed to this input are prf limited to prevent damage to the modulator. Radar Silence is a method of inhibiting transmission without using

the appropriate command in the serial message. An active signal at this input will cause the microcontroller to inhibit transmission within one trigger pulse at either of the internal prfs.

Built In Self Test (BIST)

The microcontroller performs a number of self test operations and reports the results to the Display as part of the serial message link. Error situations that are monitored in the transceiver are; serial message corruption, loss of Display messages, loss of Heading Marker signal, loss of either Charge or Modulator Trigger and spark gap arcing. Error situations will in all cases cause the microcontroller to inhibit transmission until the error has been cleared. The other signals that are monitored and sent directly to the Display without further action by the microcontroller are the power supply lines and magnetron current as described in the section on analogue inputs.

Test Modes

There are two test modes for the Trigger PCB. The production test mode is used solely during production testing of the PCB and is initiated by fitting the test link LK4. This must only be done on the production test bed as connecting this link when incorporated into a transceiver could lead to unpredictable and possibly dangerous operation.

The second test mode, of use to service engineers can be initiated by fitting the two links LK5 and LK6 to position 2-3. When in this mode the transceiver can be operated without the antenna rotating, and may be removed from the turning unit, reconnected to the Display below decks (with suitable test cables) and run as per normal operation. Fitting the links causes the Trigger PCB to generate bearing and heading marker data internally, allowing the transmitter to operate without the antenna rotating. A dummy load MUST be connected to the RF output. Since the Transceiver has been removed from the Turning Unit and the Pulse Bearing PCB outputs, the bearing and heading marker information normally required for Trigger PCB operation is simulated on a section of test circuitry on the Trigger PCB.

5.3 Transceiver Power Supply (X-Band)

5.3.1 General Information

The DC power supply is described at sub-section 5.7.

The AC power supply is an AC to DC inverter that generates the supplies for the Transceiver. The inverter is housed on a single board and is powered by an AC supply of nominal 115V or 230V in the frequency range 47-64Hz.

The power unit uses a boost converter front end to provide a regulated high voltage d.c. to 2 flyback converters providing the output supplies. Some of these supplies use additional switch mode converters to provide regulated outputs.

The outputs supplied by this power supply are:-
Variable -600V, +30V, +20V, magnetron heaters (via further regulator, +12V, -12V and +5V) and for the X-Band Turning Unit variant, +50V for the Motor Drive pcb.

The power unit has the following features:

- -600V adjustable over the range -550V to -650V for control of magnetron current via modulator.
- Output short circuit protection.
- Universal input from 95V to 276V without tap changing. Power factor corrected providing a PF of better than 0.9.

5.3.2 Functional Description (X-Band Transceiver AC Power Supply)

The following functional description is based on the block diagram given at Figure 2.27.

Principles of Operation

This power supply utilises a boost converter to provide approximately 390V d.c. to the main flyback converter which drives the power transformer T2. The principles of operation are as follows:

The incoming AC supply is filtered mainly to suppress noise emitted from the p.s.u. but also to attenuate incoming noise. Mains is then passed to the power factor controller which converts mains between 95V to 276V RMS to a stable high voltage d.c. (390V). The p.f.c. takes the form of a boost regulator which forces the input current to follow the waveshape of the input voltage as if a resistor were connected across the rectified AC supply. The p.f.c. also aims to regulate the output voltage to a level greater than the peak supply voltage. These factors are achieved by the control circuit (U3) which senses the input and output voltage as well as the input current. The control circuit sends a stream of constant frequency but varying width pulses, to the switching FET (Q1) such as to control the input current and output voltage.

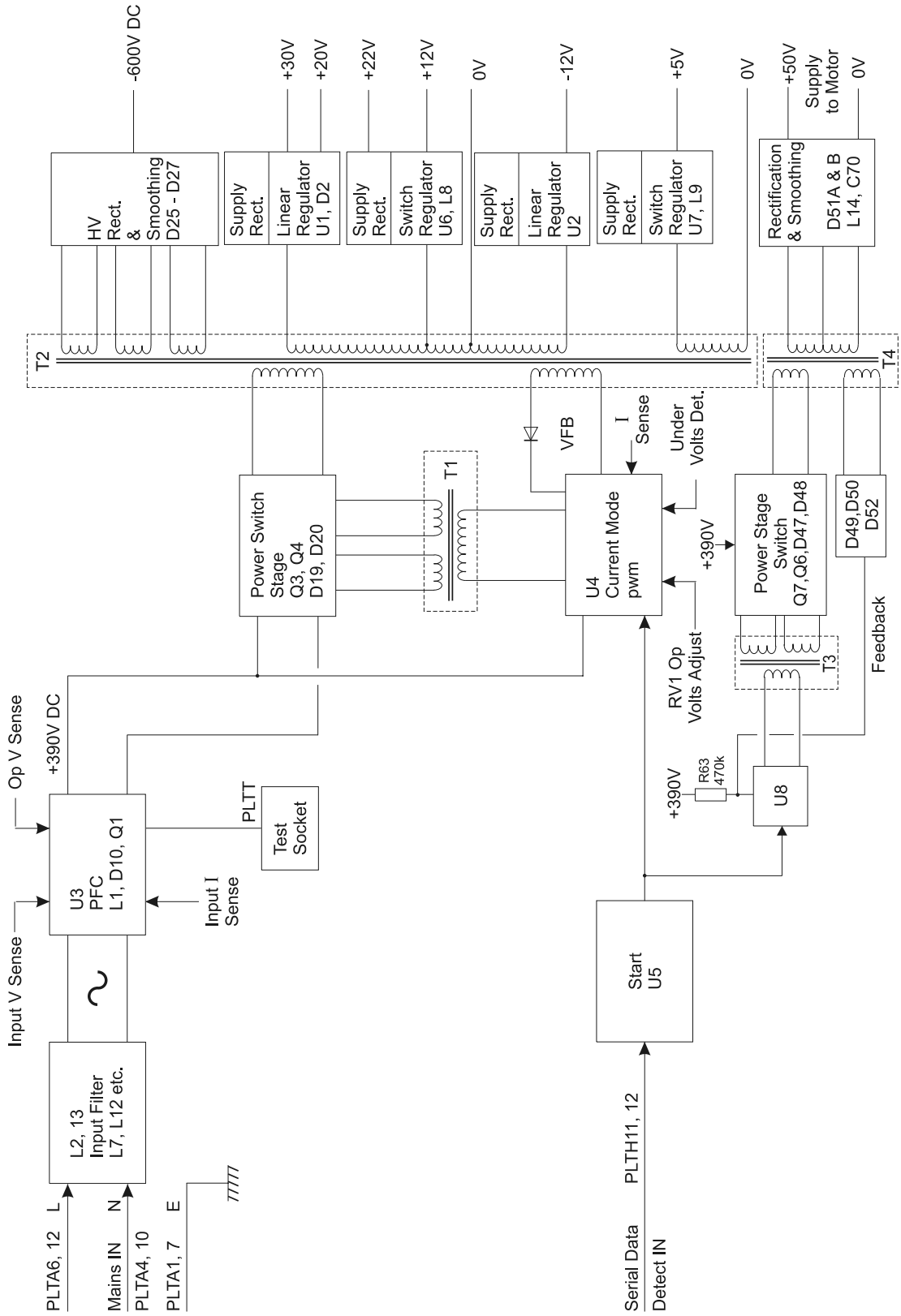

Figure 2.27 Block Diagram - AC Power Supply Board

The choke (L1) current increases during the FET on period and falls during the FET off period when the boost diode D10 conducts. This produces a triangular current waveform at 100kHz superimposed on the sinusoidal current in the choke. At full load this triangular current may be 10% of the actual peak current. The High Voltage DC (390V) is applied to the main Current Mode power converter comprising U4, Q3, Q4 and T2.

The high voltage DC line is switched to the primary of transformer T2 by the two FETs Q3, and Q4, These FETs are driven by the control circuitry (U4) such that they will both be either 'on' or 'off' together. Flyback action takes place during the off state. A small drive transformer T1 is used to provide the simultaneous but isolated drives to the two FET switches. The cross-connected diodes D19, D20 return excess flyback energy to the supply lines and provide hard voltage clamping of the FETs at a value of a diode drop above and below the supply line voltages. Switching devices with a 500V rating can be used. Energy recovery action of D19, D20 eliminates the need for an energy recovery winding or even snubbing components. Output current is fed back to U4 via sense resistor R47 which stabilised the control circuit and provides overcurrent protection under fault conditions. A further control winding provides a voltage feedback path via D32 which is used to supply power to U4 and regulate the voltage output.

DC Outputs

The following output voltages are taken from the secondary winding of T2. A series of rectifiers, reservoir capacitors, linear and switch mode regulators are connected to the secondary windings of T2 to provide the following DC voltage outputs.

1.	-600V	120mA max.	Modulator HT
2.	+30V	20mA max	Tuning Range
3.	+20V	15mA max.	Drive to IGBTs
4.	20V(approx:)	0.7A	to magnetron heaters via a switch mode step down regulator.
5.	+12v	1.5A	Rx, trigger board modulator
6.	-12V 0.6A	Rx, trigger board modulator	
7.	+5V 0	5A	Rx, trigger and pulse bearing board

An additional output (+50V @ 6A) for the Motor Supply PCB is produced from a separate switching regulator U8 and transformer T4.

As the modulator requires HT voltage that can be varied over 550V to 650V to set up the correct magnetron current, all outputs have to be further regulated to ensure stability. Adjustment of RV1 sets the required modulator HT voltage and thus the required magnetron anode current.

To produce the 600V d.c. HT, three windings on the secondary of T2 each produce 200V and are added together at the output of the rectifier circuits. The 30V and -12V rails are fed via three terminal linear regulators whilst the 20V is Zener stabilised. The +12V and +5V rails are fed via 'Simple Switchers', five terminal regulators and chokes with flywheel diodes.

The flyback current mode converter formed by U4, Q3, Q4 and T2 is started by detection

of a serial data stream applied to U5 from the display at PLTH 11, 12.On detection of the data stream the photo transistor within U5 is turned on pulling down the gate of Q2 below its threshold voltage. Q2 turns off allowing the compensation pin 1 U4 to rise enabling output of the IC U4. In the PSU off state Q2 is held on by current in R37 from Vcc.

In the absence of a serial data link from the display, for test purposes, LKA 1-2 can be made and the PSU will output the required d.c. voltages.

The operating frequency of the PFC section is approximately 100kHz. That of the PWM flyback converter is approximately 40kHz whilst the 'Simple-Switchers' run at approximately 52kHz.

Once the mains supply is applied to the PSU board, the PFC (Power Factor Correction) circuit starts and generates 390V. Whilst mains is applied, the PFC is active and cannot be manually switched off. The start circuitry only controls the flyback converter and so High Voltage DC is present on primary power components whenever mains is present on the board. **This fact should be noted when servicing the Transceiver**.

5.3.3 Circuit Description (X-Band Transceiver AC Power Supply)

The following circuit description is based on Circuit Diagram 65825916 given at Figure 2.28.

Mains Input

The AC supply enters the power supply from the external input filter via plug PLTA pins 6, 12 live, PLTA pins 4, 10 neutral and PLTA pins 1, 7 earth, to the comprehensive EMC suppression circuitry. Although the filtering provides some rejection of mains born interference its main task is to suppress pfc and main switcher interference generated from within the PSU. Due to the 100kHz triangular choke current and capacitive switching currents in the PFC power stage, common mode and differential mode interference pulses are present either side of C16. The multi-element filter formed by common mode chokes L2, L3. and differential mode chokes L7 and L12 together with the adjacent capacitors C18-C21 effectively minimise conducted 100kHz and harmonics from being superimposed on the incoming mains. VDR1 suppresses transient voltages on the AC supply whilst RT1 limits inrush currents to the smoothing capacitors C4, C5.

Power Factor Correction Circuit (PFC)

The PFC takes the form of a continuous mode fixed frequency, average current mode boost regulator. It produces a stable 390V DC rail from the incoming mains whilst ensuring the input current remains sinusoidal. The drive pulses for the main switching FET Q1 are generated by the PFC controller U3 pin 16. The ground pin 1 is referenced to HVRTN which is Q1 source and via the current sense resistors R20, 21 the bridge rectifier -ve output.

The Vcc supply for U3 pin 15 is derived from:-

1. Winding pins 7, 8 on the main choke L1.
2. Resistors R2, 3 and D31 from +HV DC
3. An external 17V dc PSU for test purposes.

All the following pins refer to U3. The V sense pin 11 senses the +HV DC (390V) line and causes Q1 drive pulses to adjust in width to keep the d.c. output voltage constant for load changes. The 0VP pin 11 senses the +HV DC line and cuts off Q1 drive if the output voltage exceeds 390V by approximately 5%. The IAC pin 6 receives a current proportional to the rectified AC voltage from the bridge rectifier D1. V ref pin 9 outputs a 7.5V reference voltage. PK lim pin 2 receives a -ve voltage from current sense resistors R20, 21 via R1. When this is large enough to take pin 2 voltage below 0V, against the current flowing through R41, Q1 drive is cut off.

The EN/SYNC pin 10 is permanently held in the enable state by resistor R19 connected to Vcc. The C set and R set pins 14 and 12 are connected to C7 and R18. These components set the frequency of the internal oscillator to 100kHz. The SS pin 13 is for slow startup which is not used in this application.

The Va out pin 7 in conjunction with components C13, C8, R14 and R13 stabilise the +HV DC feedback control circuit in U3. The M out pin 5 receives the current sense voltage via resistors R22 and R59. The I sense pin 4 senses the voltage on the HV RTN end of the current sense resistors.

Inputs on pins 4, 5 and 6 are used in U3 to control Q1 drive pulse width such as to make the average current waveform in the choke L1 follow the rectified AC output voltage from bridge rectifier D1. The CA out pin 1 in conjunction with components R23, 8, C14 and C15 stabilise the current sensing feedback control circuit in U3.

Overcurrent Limit Operation of PFC

There are two separate circuits to protect the power switching components.

a) A controlled and stable current limit circuit is built into the average current feedback control loop. The current limit value is determined by resistors R20, 21. Increasing the PFC load current above the maximum level will cause the pfc input current to progressively have a flat top to the full wave rectified waveform.

b) A second current limit path is provided by the level of voltage appearing at PKLIM pin 2 of U3. The level of this current limit point is set slightly higher than the previous one in a) above.

Start Sequence of the PFC

(with the application of mains from the ship's supply contactor).

Initially C4, C5 charge up to the peak value of the AC supply via D24, L1 and D1. Vcc line capacitor C3 starts charging via R2, R3 and D31. When C3 voltage reaches about 16V the pfc IC U3 starts operating and delivers pulses to Q1. The +HV DC starts to increase towards 390V whilst Vcc falls due to U3 current drain. The +HVDC line reaches 390V before C3 voltage drops to 10.5V where U3 would switch off. With the HVDC line at 390V, Vcc is then maintained from winding 7, 8 of L1 via D14, D15, C29 and C30.

All the time the +HVDC line is building up the current limit circuits are operating allowing the 390V line to build up in the shortest time. As the HVDC line builds up the flyback converter drive IC U4 Vcc rises. Upon reaching approximately 16V (pin 7 VCC) the IC becomes active and the power output FETs are driven. The output voltage from the power supply starts approximately 2-3 seconds from initial mains application.

Capacitors C23 and C24 serve to provide a return path for the capacitive currents resulting from stray capacities of Q1, D10 and D11 thermal insulating material on the heatsink. Prior to Q1 switching on, L1 current is passing through D10. When Q1 switches on D10 takes a finite time to switch off. At this time Q1 sees the full +HVDC voltage present on C4, C5.

A very high current pulse results causing significant power dissipation in Q1. With inductor L4 in circuit Q1 current is allowed to build up slowly until L4 saturates. At this time Q1 is switched on and its drain current has risen sufficiently to reverse D10 current. D10 turns off. This L4 circuit significantly reduces the switching losses in Q1. Diode D11 and resistors R25-R27 serve to absorb the stored energy in L4 when Q1 switches off. In particular it prevents Q1 drain voltage rising significantly above 390V.

The PFC circuit can be tested separately from the rest of the PSU by utilising the test plug PLTT. Testing the pfc is achieved by removing LKB, fitting a variac to the AC supply and applying a floating DC supply of 16 to 20V across Vcc and HVRTN (pins 4 and 5 of PLTT). The floating external PSU provides power to U3. With the low voltage supply on, the variac can be turned up whilst monitoring +HVDC. The pfc circuit should produce an output of 390V d.c. with about 4V AC input. The +HVDC line should remain stable at 390V for all IP voltages up to 276V RMS. If it rises above 390V do not increase variac input as there is a feedback fault. An external resistive load may also be connected to the pfc via PLTT pins 1, 5.

Main PWM Power Supply Stage

The pfc provides stable +390V d.c. for the current mode flyback converter over the full mains input specification. In spite of the converters dual power FETs the converter is of single ended flyback design. The high voltage DC line is switched to the primary of transformer T2 by two power FETs Q3 and Q4. These switches are driven via T1 from the control IC U4. They are both either on or off together. Drive transformer T1 provides simultaneous but isolated drive to the two FETs.

The cross coupled diodes D19, D20 return excess flyback energy to the supply line and provide hard clamping of the two FETs at a value of only one diode drop above or below the supply line voltages. In addition, energy recovery action of D19, 20 eliminates the need for an energy recovery winding or even snubbing components. This reduces the waste heat in the psu.

When both power FETs are 'on' the supply voltage appears across the transformer primary and series leakage inductance. All secondary rectifiers will be reverse biased and no secondary current flows. The primary current increases linearly and energy will be stored in the coupled magnetic field of the transformer and also energy will be stored in the leakage inductance. At the end of the 'on' period both FETs Q3, Q4 turn off simultaneously and the primary supply current in the FETs falls to zero. By flyback action all voltages on the transformer reverse. Initially clamp diodes D19, D20 conduct clamping the flyback voltage to the supply line. All output rectifiers become forward biased and secondary current flows. When the secondary current has built up (to nxIp) and the energy stored in the primary leakage inductance has been transferred back to the supply line the energy recovery clamps D19, D20 cease conduction and the primary voltage falls back to the reflected secondary voltage. Thus all surplus stored energy is recovered to the supply line and dissipation is minimised.

On application of HVDC (390V) when the mains input is first connected C55 charges up via R48. When C55 attains 16V the under voltage lockout within U4 is released and V ref is enabled and outputs 5V. Output pin 6 delivers 15V pulses to the primary of T1 and Q3, Q4 receive in phase drive pulses which in turn causes primary current to build up. Primary current is sensed across R47 and fed back to pin 3 U4 for feedback stability and overcurrent detection. Voltage feedback is generated from windings 10, 50 from T2 via resistor network formed by R31, R32, R33 and RV1 into pin 2 U4. frequency compensation for the error amps within U4 is accomplished by network formed by C53, R30. In addition to providing voltage feedback the feedback winding (10, 50) supplies power to U4 via D32 and C55 once the psu has started operating and supplying output power. The feedback voltage as applied to pin 2 U4 is adjustable via RV1 which sets the raw output voltage levels of all secondary windings.

Overcurrent trip operation occurs should the primary current exceed 4.5A approximately. Once I sense pin 3 (U4) exceeds 1V then the gate drive output ceases and the feedback voltage falls. Once the feedback voltage on pin 7 (U4) falls to less than 10V the V ref shuts down and C55 discharges. The only charge path for C55 now is R48 and after approximately 1-2 seconds C55 exceeds 16V and output pulses are initiated and the PSU operates.

Should a permanent short circuit be applied to one of the power output lines the psu will 'hiccup' continuously with an approximately 3 sec off time. Thus the mean power dissipated within the psu under fault conditions should be low. Gate drive is clamped by D21, 22, 17 and 18 so as not to exceed the FET gate voltage specification. R49, 50 serve, together with the FET gate capacitance, to slow the switching edges of the power drain waveform thus minimising conducted and radiated interference without causing excessive power dissipation within the FETs.

To switch the flyback converter on the opto-coupler detects the presence of a serial data stream from the display at PLTH 11, 12. On detection of the data stream the photo transistor within U5 is turned on pulling down the gate of Q2 below its threshold voltage. Q2 turns off allowing the compensation pin 1 U4 to rise enabling output of the IC U4. In the PSU off state Q2 is held on by current in R37 from Vcc. For test purposes the PSU can be turned on in the absence of a serial data stream by linking 1-2 on LKA.

T2 Secondary Circuits

Modulator -600

The three isolated windings of T2 (1-20, 2-19, 3-18) are individual 200V windings each having a rectifier and reservoir capacitor. The supplies are connected in series to give the required -600V supply for the modulator.

Receiver Tuning Supply +30V

Rectifier D9 and capacitor C41 provide d.c. input to the three terminal linear regulator U1 which produces a fixed 30V output. L5 and C10 provide additional noise filtering.

Modulator IGBT Drive Supply +20V

Zener stabilisation formed by D2 and R15 converts +30V input to a stable 20V supply using L6 and C39 as additional noise filters.

Magnetron Heater Supply

D28 together with C31, 32 provide approximately 20V d.c. for the magnetron heater switch mode regulator on the modulator pcb.

Rx/Trigger Board +12V

With approximately 20V input from D28, C31, and C32 the five terminal 'Simple Switcher' U6 output is set to +12V by R52, R53 and R54. The switcher operates at approximately 50kHz using L8 as the step down regulator inductor and D3 as the flywheel diode. Whilst the power device within U6 is off energy is transferred to the load via L8 and D3.

Rx/Trigger Board -12V

D12, C33 provides approximately 20V d.c. into the three terminal linear regulator U2. R16, R17 set the output of U2 to -12V.

Rx/Trigger Board +5V

D29, C44 provide approximately 15V d.c. to the input of U7 a 5 terminal 'Simple Switcher' power IC. R55, R56 sets the output of U7 to 5V. L9 supplies power to the load, during the off period of U7, via D7. This simple switcher operates at approximately 50kHz.

All output linear regulators are protected against input short circuits by reverse diodes connected from output to input (D8, D6). Both linear regulators and simple switchers are current limited for short circuit protection.

T4 Motor Supply Output

On application of HVDC (390V) when the mains is first connected, C73 charges up via R63. When the voltage on C73 attains 16V the under voltage lockout within U8 is released and V ref is enabled and outputs 5V. Output pins 11 and 14 deliver 15V pulses to the primary of T3. Power Mosfets Q6, Q7 receive out of phase drive pulses which in turn causes primary current to build up. Q6, Q7 and capacitors C4, C5 form half bridge power stage. Capacitor C69 AC couples the power switch signal to the power transformer T4. This minimises the possibility of core saturation in T4. Diodes D45, D48 are incorporated to ensure that the integral Drain/Source diodes within the power Fets do not conduct during voltage reversals in the Fet switch off periods. Primary current is sensed across by T5 and fed back to pin 9 U8 for feedback stability and overcurrent detection. Voltage feedback is generated from windings 10, 9 from T4 via D49, D50 and L13 to pin 1 of U8 via R79.

The feedback voltage as applied to pin 1 U8 is set via the ratio of R79 and R65 which sets the output voltage level of secondary windings 5, 6 of T4 to a nominal 50V. Frequency compensation for the error amps within U8 is accomplished by a network formed by C72, R80, R78 and R65. In addition to providing voltage feedback the feedback winding (10, 9) supplies power to U8 via D49, D50, D52 and C65 to pins 13 and 15 once the PSU has started operating and supplying output power.

Overcurrent trip operation occurs should the primary current exceed 1.5A approximately. Once ILIM pin 9 (U8) exceeds 1.2V then the gate drive output ceases and the feedback and output voltage falls. Once the feedback voltage on pin 15 (U8) falls to less than 10V the V ref shuts down and C65 and C73 discharge. The only charge path for C73 now is R63 and after approx 1-2 seconds C73 exceeds 16V and output pulses are initiated and the PSU operates.

The Motor supply output (+50V) is derived from windings 5, 6 of T4 via D51A/B, L14 and C70. R77 and C71 perform noise suppression of switching edges. A train of pulses is produced from the rectifying diodes D51A,B, the mean DC level of which is controlled by the ratio of the on to the off period. By varying the mark-space ratio, the mean DC level at the output of the low pass filter, formed by L14 and C70, can be controlled to the required level.

Should a permanent short circuit be applied to the power output line the psu will 'hiccup' continuously with an approximate 3 sec off time. Thus the mean power dissipated within the psu under fault conditions should be low. Gate drive is clamped by D34, 35, 36 and 37 so as not to exceed the FET gate voltage specification. R74, 75 serve, together with the FET gate capacitance, to slow the switching edges of the power drain waveform thus minimising conducted and radiated interference without causing excessive power dissipation within the FETs.

To switch the half-bridge converter on, the opto-coupler U5 detects the presence of a serial data stream from the display at PLTH 11, 12. On detection of the data stream the photo transistor within U5 is turned on pulling down the gate of Q5 below its threshold voltage. Q5 turns off allowing the soft start pin 8 U8 to rise enabling output of the IC U8. In the PSU off state Q5 is held on by current via R37 from Vcc. For test purposes the psu can be turned on in the absence of a serial data stream by linking pins 1-2 on LKA.

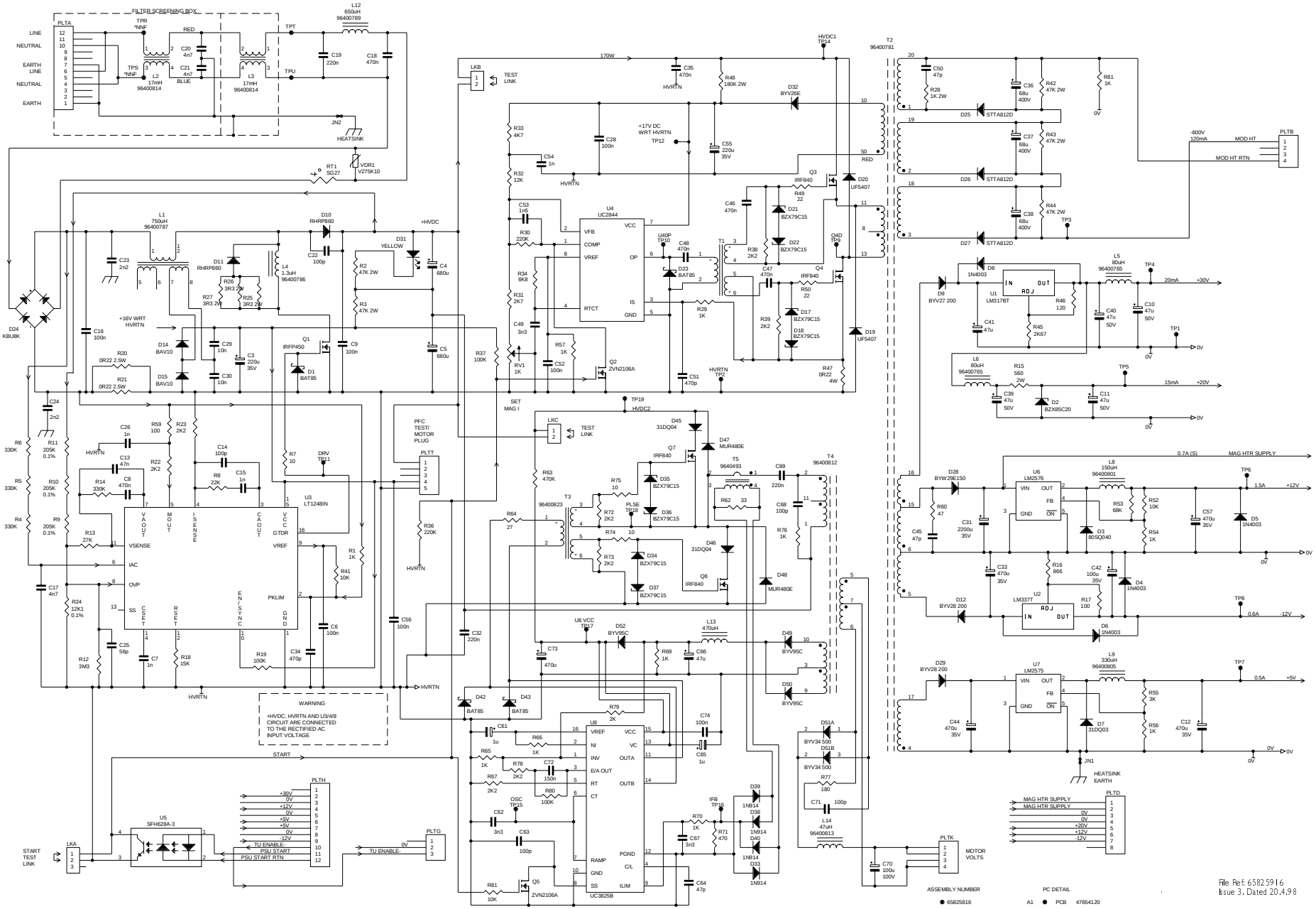

Figure 2.28 Circuit Diagram 65825916 - X-Band Transceiver Power Supply

A3 page 2-59/60 Figure 2.28, discard this A4 sheet.

5.4 Modulator PCB (X-Band)

5.4.1 Functional Description

The principal function of the Modulator PCB is to generate an 8kV, 8A negative pulse to drive the cathode of the magnetron. An SCR is used to resonantly charge a Pulse Forming Network (PFN) to -1200V from the -600V Modulator HT supply. The charging cycle is initiated by the Charge Trigger. The number of sections of the PFN is selectable by the relays controlled by the Pulse Length Control Lines. The number of sections of the PFN used defines the length of the output pulse.

At a defined time after the PFN is fully charged it is discharged by three series connected Insulated Gate Bipolar Transistors through a pulse transformer. The discharge is initiated by the Modulator Trigger. The Pulse Transformer, which has step up ratio of 12:1, transforms the resulting pulse to 8kV. The back edges of the medium and short pulses are speeded up by a saturable reactor connected across the primary of the pulse transformer.

Other functions include regulating the magnetron heater supply, monitoring a spark gap to ensure correct operation of the magnetron, and generation of a timing reference for the Radar Trigger.

5.4.2 Inputs to the Modulator PCB

-600V Modulator HT Supply
+20V Modulator Trigger Supply
+16V - +27V Magnetron Heater Bulk Supply
+12V
-12V

Short Pulse Control Line	when 0V selects short pulse.
Medium Pulse Control Line	when 0V selects medium pulse.
Charge Trigger	initiates charging of Pulse Forming Network. Typically 1Amp current pulse.
Modulator Trigger	initiates discharge of Pulse Forming Network. Typically 4us, 3.5V positive pulse.
Turn Down Enable	dc voltage controls the magnetron heater voltage. 0V on long pulse, 3.5V Standby Medium and Short Pulse

5.4.3 Outputs from the Modulator PCB

Primary sample	positive pulse sample from pulse transformer used to initiate Radar Trigger. Typically 40V amplitude.
Magnetron current sample	a dc voltage proportional to the magnetron current derived from the secondary of the pulse transformer. Typically +2.5V (on long pulse).
TX Active	a signal that is normally 0V that rises to >2.5V if the spark gap operates continuously for 2 seconds. This signal is used by the Trigger PCB to indicate a transmitter fault to the display.

HT Sense	sample of Modulator HT Supply fed to Trigger PCB for inclusion in BITE message sent to display.
TX Define	Link settings used to define modulator type to Trigger PCB. 0V or 3.5V dependant on link settings.

5.4.4 Circuit Description (X-Band Modulator PCB)

The following circuit description is based on Circuit Diagrams 65810912 (X-Band 10kW Modulator PCB) Figure 2.29, and 65825912 (X-Band 25kW Modulator PCB) Figure 2.30.

Magnetron Heater Supply

The magnetron heaters are derived from the Magnetron Heater Supply at PLVD1 and PLVD2. This supply may vary between 16V and 27V.

The Modulator PCB is configured for the intended magnetron by the setting of link LK1 fitted to the Modulator PCB. Refer to Figure 6.38 'Link Settings - Modulator PCB', in Chapter 6, for further information.

WARNING - On no account should the heater voltage be measured whilst the Transceiver is transmitting.

In a 10KW X-Band system, the magnetron requires a heater voltage (measured between TSJ1 and TSJ2) of 6.1V on Standby, Short Pulse, Medium Pulse and Long Pulse.

In a 25KW X-Band system, the magnetron requires a heater voltage (measured between TSJ1 and TSJ2) of 6.1V on Standby, Short Pulse, and Medium Pulse. On Long Pulse, this may be turned down to 5.1V depending on the type of magnetron fitted.

The Mag Heater Supply is connected to the input of the switching regulator U1. U1 is configured as a buck regulator running at a constant frequency of approximately 52kHz. During the time that the regulator is switched on, power is supplied to the load from the Mag Heater Supply via L106. When the regulator switches off, energy stored in L106 is transferred to the load via commutation diode D112. C112 provides output smoothing. The output voltage is sampled by the feedback network R132, R133, R145, R136, and Q102. The sample voltage is fed back to pin 4 of U1 where it is compared with an internal voltage reference. If the sample voltage fed back is greater than the internal reference voltage the time that the regulator is switched on for is reduced until the sampled voltage equals the reference voltage. Similarly if the sample voltage is less than the internal reference voltage the time that the regulator is switched on for is increased until the two voltages are equal. In this way a constant output voltage can be set by selecting values in the feedback network.

When long pulse is selected, the Turn Down Enable signal at the gate of Q102 is 0V biassing Q102 off. In this condition R136 is connected in series with the feedback network, increasing the voltage at U1 pin 4. The regulator 'on' time is therefore reduced and the output voltage is reduced to the level required for 5.0V magnetron heaters.

When Standby, Short Pulse, or Medium Pulse is selected the Turn Down Enable signal at the gate of Q102 is set by the Trigger PCB to 3.5V turning Q102 on. When Q102 is turned on, R136 is short circuited and the voltage at pin 4 of U1 is reduced.

The regulator 'on' time is therefore increased and the output voltage is increased to the level required to set the magnetron heaters to 6.3V. The inductor L103 and capacitor C115 isolate the regulator from the high voltage pulse that appears at the bias winding of T107. The voltage at the output of the regulator measured at TP106 is typically 1.5V greater than the 6.3V or 5.0V to allow for the voltage drop across L103 and the secondary of the Pulse Transformer.

Charging the PFN

With -600V supplied from the Power Supply PCB via L101, the PFN charging is initiated by the positive edge of the Charge Trigger signal on PLVC8. This trigger signal passes via the isolating transformer T101 to the gate of input SCR Q101. The positive pulse turns the SCR on to start the resonant charge. Because L101 and the capacity of the PFN form a resonant circuit, the input current to the PFN is sinusoidal in character and the line charges to about 1.8 times the Modulator HT supply voltage.

The PFN charges through Q101, the isolating diode D101, and the delay reactor L105. The charge current reaches a peak and decays to zero, and at this point D101 becomes reverse biassed and Q101 turns off. This occurs when the voltage on the PFN is at its maximum value. R106, R107, and R108 provide a discharge path for any voltage on the anode of Q101. R126, R129, R130, and R131 form a potential divider across the Modulator HT Supply to feed a sample voltage to the Trigger PCB for incorporation into the BITE message sent to the display.

Discharging the PFN

The modulator is triggered by the Modulator Trigger pulse from the Trigger PCB. This positive pulse of typically +3.5V amplitude is amplified to 20V by U3, . The output of U3 is fed to the primary of the isolating transformer T105. The transformer has three identical secondary outputs, each of which drives one of the gates of the series connected IGBT's Q103, Q104, and Q105. The transformer turns ratio is 1:1 so each gate emitter of the IGBT's is driven by a 20V positive pulse.

By clamping any signals fed back from the transformer to a safe level, D111 and D110 protect the output of U3. R121, R122, and R123 control the peak current spike into the capacity of each gate to ensure the IGBT's turn on together. Initially the delay reactor L105 is high impedance and momentarily delays the discharge of the PFN until the IGBT's are fully turned on. This ensures that high current does not flow through the IGBT's until the voltage across them has fallen to a low level. Approximately 250nS after the trigger pulse the delay reactor saturates, and the PFN is discharged through the primary of the Pulse Transformer T107. The resulting 650V primary pulse is transformed up to 8kV to drive the magnetron.

D107 in the charging circuit clamps any positive spike fed back through the capacity of D101 to protect Q101. R125, R126, R127, VDR1, VDR2, and VDR3 ensure that the voltage is shared equally across each IGBT.

Defining the Pulse Length

The PFN defines the transmitted pulse shape. It is only when long pulse is selected that all the energy stored in the PFN is transferred to the magnetron. On medium and short pulse the transmitted pulse length is controlled in two places, using RL1 and RL2.

a) The PFN
The relays are used to select the number of sections of the PFN that are used for a given pulse length. The more sections used, the longer the pulse.

b) The Tailbiter.
On short and medium pulse the PFN is used to define the start of the pulse but the width of the pulse is determined by a saturable reactor L104 (tailbiter) connected directly across the primary of the pulse transformer. The number of turns on L104 is varied to suit the pulse length required. The number of turns is selected by RL1 and RL2 dependant on the pulse length selected.

The tailbiter acts by changing from a high impedance to a low impedance to short circuit the primary of T107, terminating the drive pulse to the magnetron. The time that L104 remains in the high impedance state is dependant on the number of turns and the voltage impressed across it. Any charge remaining in the PFN when L104 changes state, is dumped into the circuit consisting of D102 and R115. The PFN is then in a fully discharged state ready for the next charging cycle.

Pulse Length	Relay Energised	PFN Capacitors in Circuit	L104 Tailbiter Winding Used
Long	None	All	None
Medium	RL2	C105, C107, C108 C109	1 - 3
Short	RL1	C105, C107	2 - 3

Relay 1 and Relay 2 Operation

Pulse Transformer

The purpose of the Pulse Transformer T107 is to match the impedance of the PFN to the impedance of the magnetron. In doing this, it also steps up the voltage pulse to the correct level to drive the magnetron. The output of the PFN is directly connected to the primary of the Pulse Transformer, and the secondary is connected directly to the magnetron cathode. A bifilar wound secondary is used to allow the heater supply to be connected to the magnetron. An additional secondary winding carrying the heater current is used to bias the core of the transformer magnetically, so that the number of secondary turns required to support the long pulse voltage pulse can be kept to a minimum.

R137 and current transformer T108 in series with the primary of T107 provide a 40V positive pulse (Mag Sample) to the Trigger PCB as a timing reference for the Radar Trigger, and AFC Trigger.

R119, D104, C118, R118, and current transformer T106 in series with the Pulse Transformer secondary provide a rectified output (Mag Current Sense) proportional to the magnetron current. This voltage is passed to the Trigger PCB where it is incorporated into the BITE message sent to the display.

Zener diode D127 restricts the maximum output voltage below the level that would damage the circuit on the trigger PCB. The voltage can be monitored at TP100, and is used to set the magnetron current in service.

The EHT PCB

The two leads from the bifilar secondary of the Pulse Transformer are routed through the EHT PCB. D106, D113, and R120 clamp any positive overswing at the end of the magnetron pulse and absorb any surplus energy from the secondary of the Pulse Transformer. The spark gap (Gap 1) operates at approximately 12kV and provides protection for the Pulse Transformer if the magnetron mistriggers, or if the magnetron heaters become disconnected.

Spark Gap Detection Circuit

The earth return for the Spark Gap is routed through current transformer T104. When the Spark Gap operates the current through T104 generates a positive pulse across R138. This pulse is used to trigger monostable U4A. D124 and D125 clamp the input voltage to the monostable to a safe level. The resulting positive pulse at the "Q" of U4A charges capacitor C125 positively. The voltage at C125 +ve rises from its normal value of 0V towards +12V. This voltage is sampled by the Trigger PCB, and when the voltage rises to +2.5V the Transceiver is switched to standby and an error message is sent to the display.

On long pulse the spark gap has to be triggered for approximately two seconds for the voltage on C125 +ve to reach 2.5V. R143 provides a discharge path for C125, which discharges between monostable pulses such that the voltage on C125 returns to its normal level in approximately four seconds if there is no spark gap activity.

R139 and zener diode D122 provide a 3V bias for the electrolytic capacitor. Zener diode D126 together with D122 restrict the maximum voltage at C125 +ve to 4.5V. R147, R148 and D120 ensure that the voltage at C125 +ve is always positive. These limits are required to protect the circuitry on the Trigger PCB. Low leakage diode D121 prevents C125 discharging through the output of U4A.

5.5 Motor Drive Board (X-Band) (Incorporating the Dynamic Brake facility)

The Motor Drive PCB generates the supply and control signals for the 3-phase electronically commutated DC motor that turns the Scanner Unit. The Motor Drive PCB has the capability of providing High and Low speed operation by link selection on the PCB.

5.5.1 Circuit Description (X-Band Motor Drive Board)

The following circuit description is based on Circuit Diagram 65801911 given at Figure 2.31.

The Motor Drive pcb is supplied with +50VDC and +12VDC from the Transceiver power supply (in both Aloft and Bulkhead fits). There is extensive protection provided in case either of the supplies fails. This is necessary because the output driver stage is supplied from the +50VDC side, and the control signals are generated on the +12VDC side. R51,R52 and D13 prevent the slow start voltage across C27 from rising until the +50VDC supply is valid.

Pulling control line 'TU Enable' below 1.5 volts starts the voltage across C27 rising which in turn allows a slow build up of speed up to the maximum set by the speed selection link. The 6 complementary output FET switches (Q7-Q12) which perform the commutation, are protected by a current sensing and limiting circuit, in the event of overload or stall. The current sensing elements are 2 thick film resistors in parallel (R19 & R25). Note that it is possible for the circuit to function with one of these open circuit, however, the maximum load current available will be halved.

A voltage reference of +5V is generated inside the motor control IC (U1) and is available at pin 2 (VREF). This is used to generate the speed control voltage at pin 1 (E/A IN+) via a resistor divider network and speed setting link LK1.
The basic "chopping" frequency of 10KHz is defined by R22 and C15 and appears as a small sinusoidal waveform on pin 25 (RC OSC).

A second +5VDC supply (+V sensor) is generated on-board by voltage regulator U2 and supplies power to the Hall position sensors within the motor, and to the associated pull-up resistors R26,27,28.

Signals from the Hall Sensors in the motor are used to control the commutation sequence, and are also used to provide a degree of speed compensation in high wind load conditions.

An additional feature of the PCB is a Dynamic Brake which limits the 'windmilling' speed of the Antenna when the radar is turned-off, or is in Standby mode. This circuit is passive and will operate with no supply voltage. The back E.M.F of a windmilling motor turns on Q13 via D7 which then activates power FET Q14. This shunts the motor current via R42 (thick film resistor) to ground. The voltage developed across R42 is sensed by Q16 and will turn off Q14 if the current exceeds approximately 6 Amps. In effect, this forms a fast acting switching load across the motor supply when the motor back E.M.F exceeds the supply voltage by approximately 1V.

5.6 Input Boards (X-Band)

The following circuit diagrams are also included.

Circuit Diagram 65801913 - X-Band Masthead Input Board - Figure 2.32
Circuit Diagram 65801920 - X-Band Bulkhead Input Board - Figure 2.33

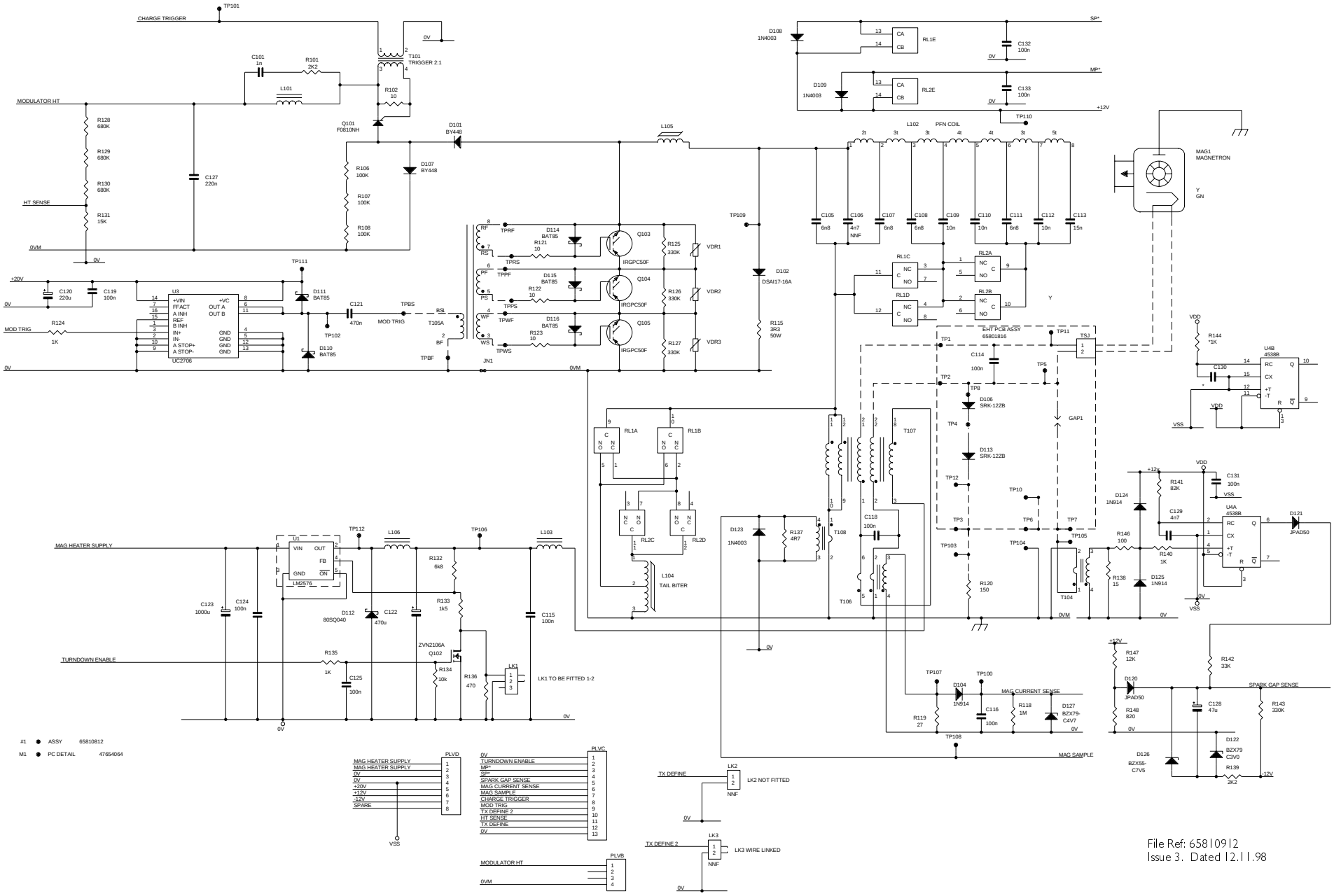

Figure 2.29 Circuit Diagram 65810912 - X-Band Modulator Board (10kW)

A3 page 2-67/68 Figure 2.29, discard this A4 sheet.

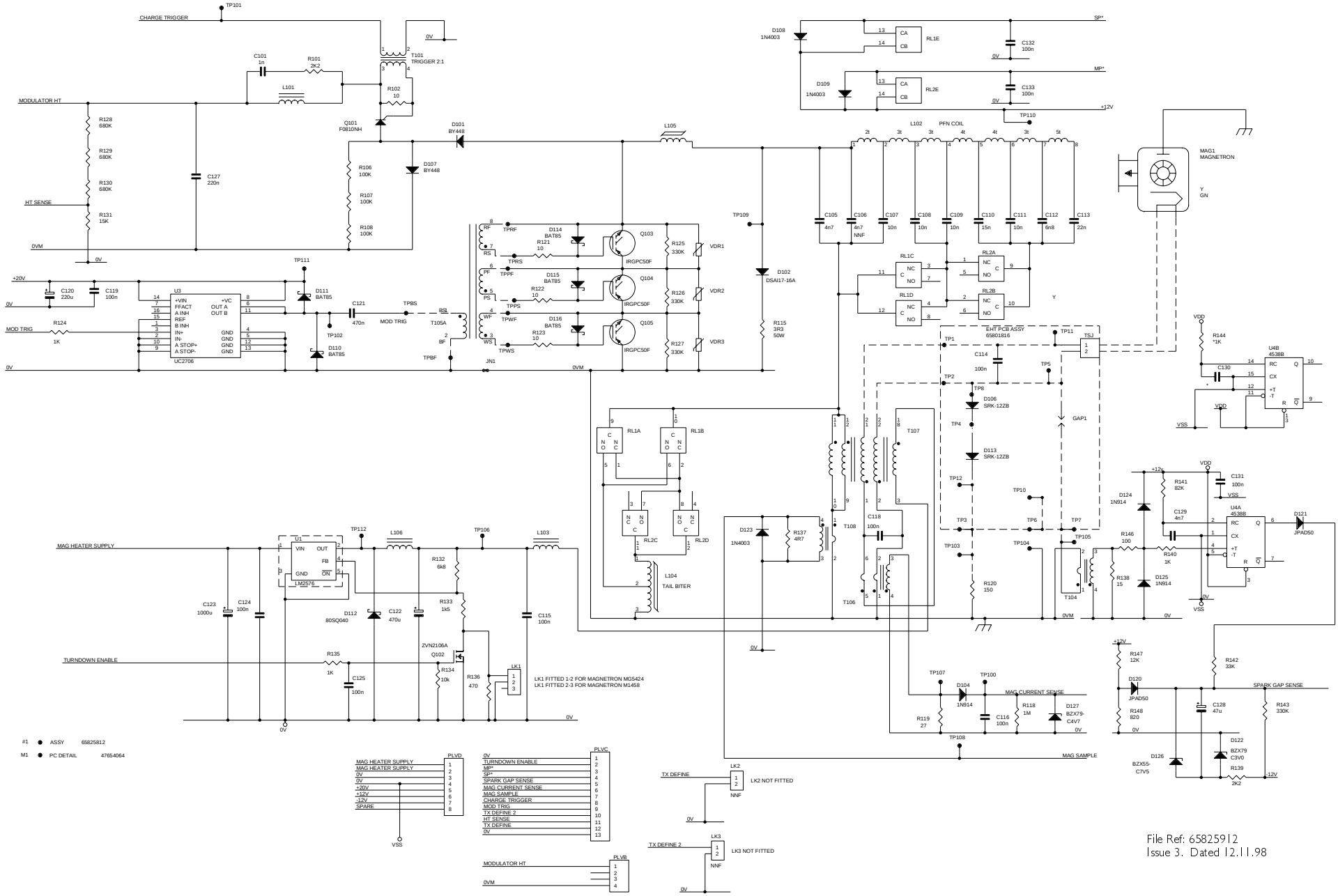

Figure 2.30 Circuit Diagram 65825912 - X-Band Modulator Board (25kW)

A3 page 2-69/70 Figure 2.30, discard this A4 sheet.

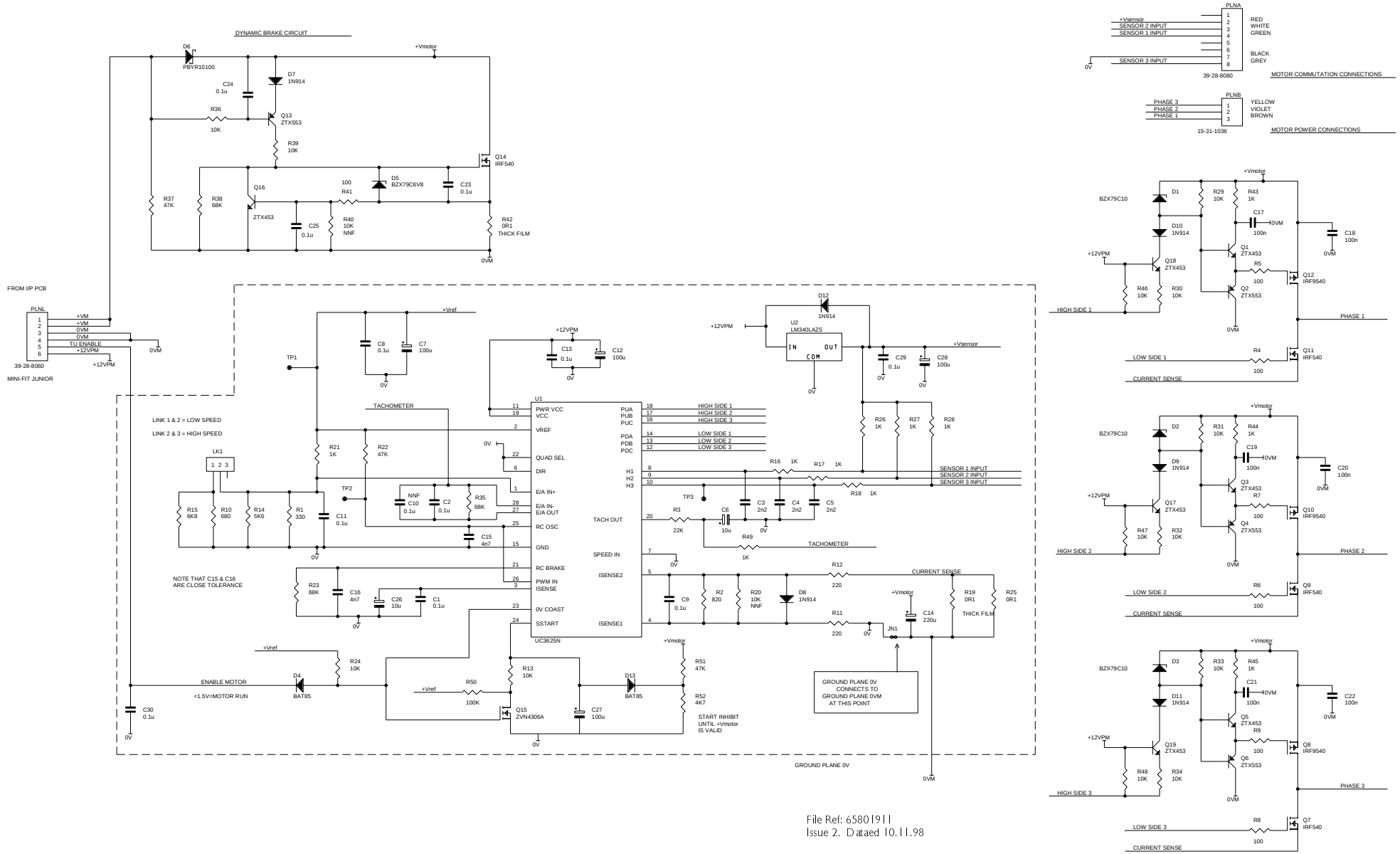

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Figure 2.31 Circuit Diagram 65801911 - X-Band Motor Drive Board

A3 page 2-71/72 Figure 2.31, discard this A4 sheet.

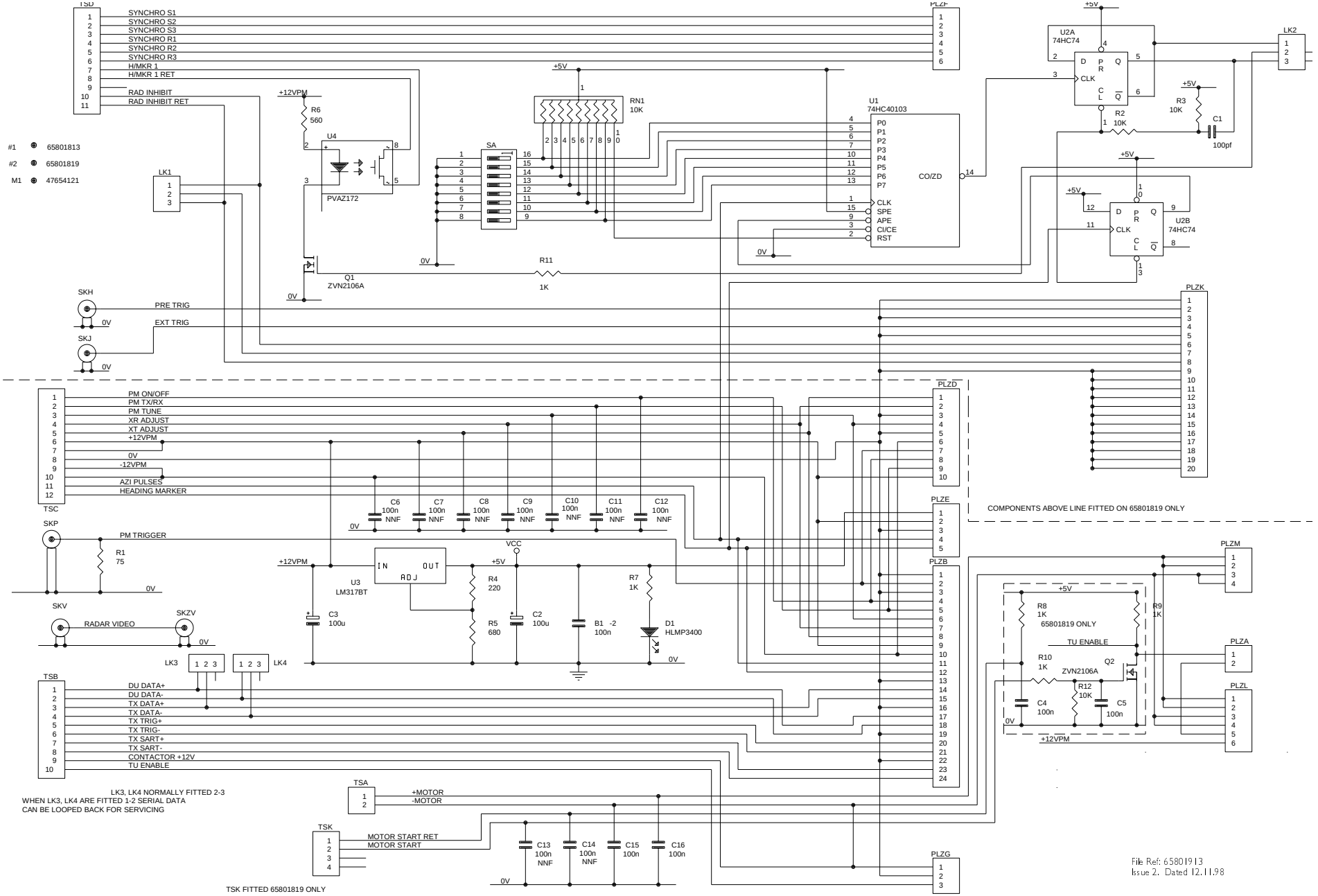

Figure 2.32 Circuit Diagram 65801913 - X-Band Masthead Input Board

A3 page 2-73/74 Figure 2.32, discard this A4 sheet.

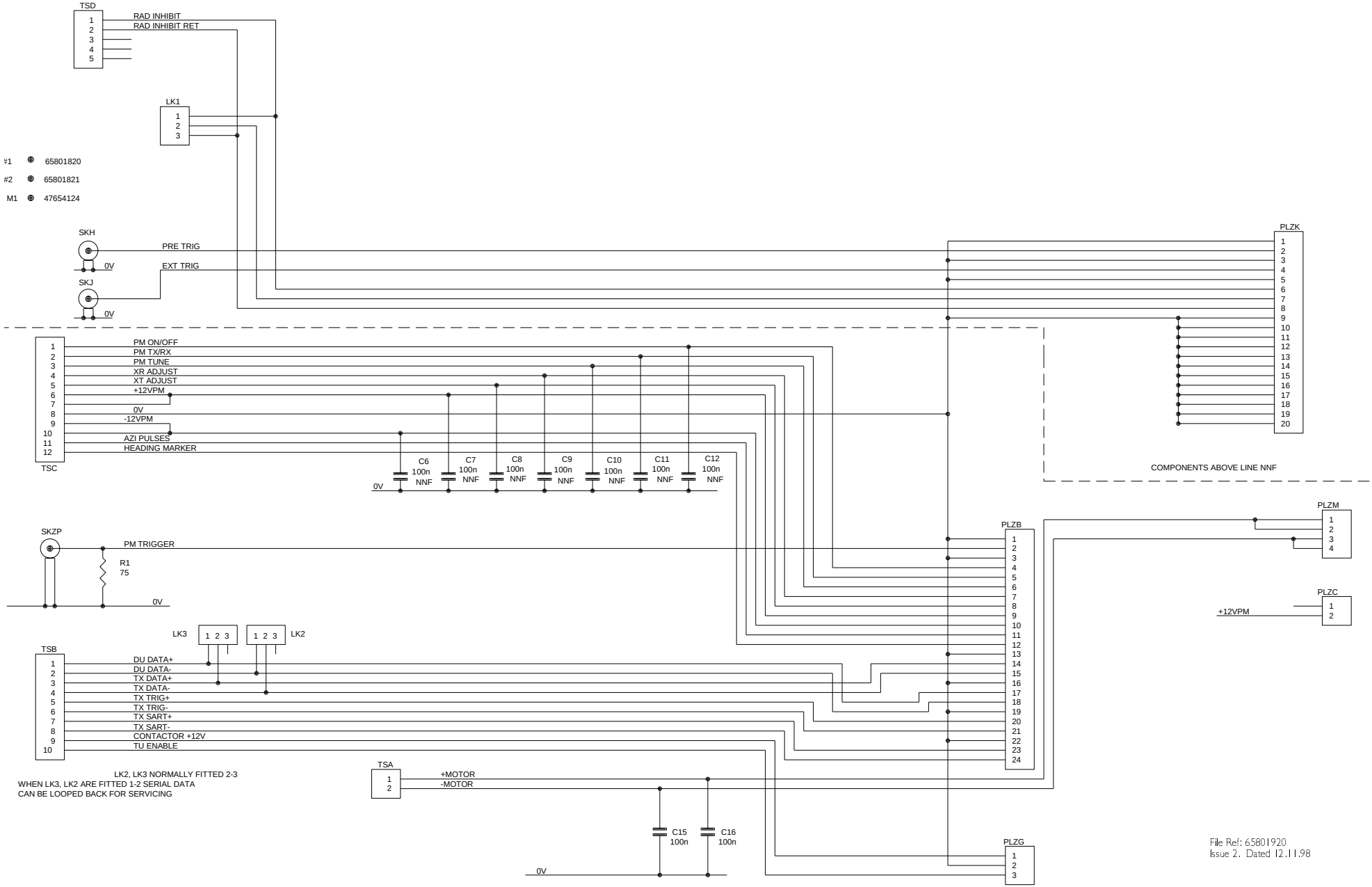

Figure 2.33 Circuit Diagram 65801920 - X-Band Bulkhead Input Board

A3 page 2-75/76 Figure 2.33, discard this A4 sheet.

5.7 Transceiver DC Power Supply (X-Band)

5.7.1 General Information

The power supply unit is of dual converter design that generates the supplies for the X-Band Transceiver. The converter is housed on a single board and is powered by a DC input of between 21.6V and 32V.

The power unit uses a push-pull converter front end to provide regulated high voltage d.c. to a flyback converter providing the modulator HV d.c. +30V and +20V. The push-pull converter supplies ±12V, +5V and motor volts of 50V either directly or via 3 terminal regulators.

The PSU has the following features:-

- Adjustable HT voltage for control of magnetron current via the modulator.
- low and high input voltage protection.
- Reverse polarity protection for the d.c. input.
- Output short circuit protection.
- Slow start for controlled run up.

5.7.2 Functional Description (X-Band Transceiver DC Power Supply)

The following functional description is based on the block diagram given at Figure 2.34.

Principles of Operation

The PSU takes the form of a d.c. – d.c. converter using a pair of power FETs driven alternately to switch the ship's supply into the primary winding of the power transformer. Voltages induced in the secondary windings are rectified, filtered and the +5V and ±15V are further regulated to provide the d.c. outputs. The push-pull converter also produces +140V for the flyback converter which generates the modulator HV. In addition, this converter produces +30V for tuning and +20V for IGBT drive.50v is generated for aerial motor rotation.

Stabilisation of the outputs and regulation against variation in the supply voltage are carried out by a regulating pulse width controller. The pulse width is governed by the level of the input voltage and the output load current. Higher input voltage tends to reduce the pulse width whilst higher load currents tend to increase the pulse width. The switching frequency remains constant.

Pulse width control is achieved by using a signal derived from a +15V feedback winding isolated from the output voltages but referenced to the ship's d.c. input. This potted down signal is routed back to the error amplifier within U6. A proportion of the feedback voltage is compared with a stable reference voltage and the output of the error amplifier is compared with a signal representing the slope of primary current in T1.

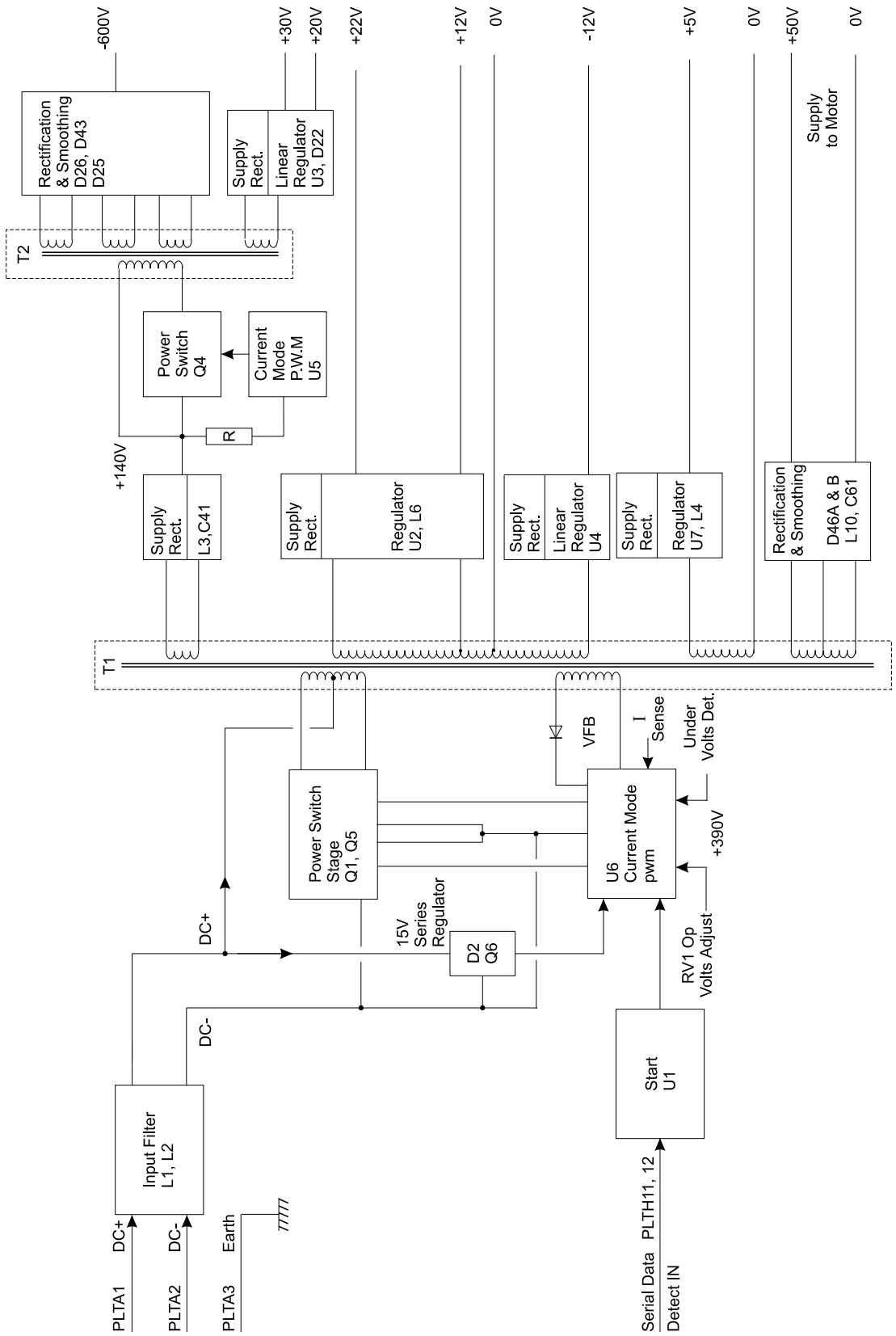

Figure 2.34 Block Diagram - DC Power Supply Board

The output of the comparator is thus a varying pulse width depending on both the primary current and feedback voltage. Input under-voltage protection is achieved by comparing an attenuated version of the input voltage with the reference voltage of U1A. If the supply input drops below approximately 17V d.c. the output of U1A goes low causing the PSU to shut down. When the ship's d.c. returns to within the normal operating range the PSU soft starts.

The input over-voltage protection circuit operates by monitoring the ship's d.c. supply using a zener diode (D7). If the input exceeds approximately 35 volts the controller U6 is shut down. Returning the input voltage to normal limits automatically re-starts the PSU. The current sense transformer (T3) feeds the attenuated primary current signal into both the p.w.m (current mode port) and the overcurrent latch circuit formed by U1C, Q2 etc. The current mode controller (U6) also terminates output pulses should the primary current exceed a preset limit. Thus there are two paths of overcurrent shutdown.

Common mode and differential mode filtering is provided at the input to the PSU. Reverse voltage protection is also provided which if it should occur would blow the input fuse.

Starting the p.s.u. is by detection of the presence of serial data at PLTH by U8. This enables the p.w.m. in U6 via U1B.

DC Outputs

The power supply outputs the following voltages:-

- variable modulator HT adjustable over the range –550V to –650V.
- +30V tuning
- +20V IGBT drive
- +50V aerial motor
- +16V magnetron heater circuit
- +5V trigger board and ±12V trigger board

5.7.3 Circuit Description (X-Band Transceiver DC Power Supply)

The following circuit description is based on Circuit Diagram 65810816 given at Figure 3.35.

Input Supply

The ship's d.c. supply enters the PSU via PLTA to the input filter consisting of C1 – C3, L1 and L2. Transient filtering is performed by VDR1 a zinc oxide voltage dependent resistor. The input filter is effective against line to line and line to ground interference. Diode D1, connected across the d.c. input protects the PSU against reverse polarity input. If this should occur the diode will conduct and short out the supply blowing the input fuse. Q6, D2 and D51 form a 15 volt series regulator.

This forms the start up supply to the p.w.m. controller U6. After the PSU has started the supply is derived from the feedback winding via D52.

PWM Control Circuitry

The p.w.m. driver provides two out of phase pulse width modulated waveforms to the gates of the power switching FETs Q1 and Q5. The FETs are turned on alternately for periods of time dependent on the output voltage and load current. T1 primary winding current is sampled via T3 and fed to the pulse by pulse limiting circuit within U6 (pin 4) and overcurrent latch circuit (U1C, Q2). D14-17 rectify the attenuated primary pulse from T3 and supply a voltage proportional to primary current to pin 8U1C. In comparator U1C a proportion of the reference voltage (0.9V derived from 5.1V) is applied to the non-inverting pin 9 U1C. Should the primary current exceed 0.9V at pin 8 U1C the output of U1C goes low pulling down the base of Q2.

The collector of Q2 rises to the 5.1V ref causing D18 to become illuminated. By positive feedback pin 8 U1C goes further positive which latches U1C. The high signal from Q2 collector is also fed via D18 and R16 to pin 16 U6 to initiate shutdown. The latched overcurrent state can only be reset by interrupting the serial data stream to U8.

At switch off, the current trip latch U1C and Q2 are reset by the low output from U1D. Latching occurs in less than 100ms to minimise the number of fault current pulses handled by the FETs. Each time that the drive waveforms are re-started from either interruption of the serial data or overcurrent operation the slow start current comprising R56, R59 and C55 comes into operation.

Over Current Protection

With current mode regulation, peak current sensing automatically provides flux balancing in push-pull converters and minimises the chance of transformer saturation due to asymmetrical drive. In addition, by limiting the peak swing of the error amplifier an instantaneous peak current limit is provided. By controlling the voltage at I LIM (pin 1U6) the peak current in the primary can be controlled.

The peak-peak current limit circuit is of the hiccup mode with auto-reset. The inter-pulse period is of one to two seconds and should operate prior to the latching overcurrent circuit. The snubber network formed by R6, C10 limit the voltage excursions caused by the interruption of current in T1 by FET turn off and absorb leakage inductance energy. The input capacitors C9, C65, C66 provide pulse to pulse energy for the output stage and ensure that the output stage remains stable under all conditions of load.

The switching aid network (D4, R4, R45. R65 and C6) across Q5 and a similar network across Q1 reduce the drain/source over-voltage transient at turn off.

U6 operates at a fixed frequency of approximately 80kHz set by R57 and C54. An internally generated 500ns blanking pulse is applied to the outputs at the end of each pulse to provide a dead time for recovery of output rectifiers and to ensure the power pulses do not overlap. The oscillator ramp is buffered by Q3 and the signal is mixed with the current sense ramp and applied to pin 4, U6. This ensures stability of the power supply at duty cycles of greater than 50%.

Under Voltage Protection

Under voltage protection (IP) is provided by U1A. The raw ship's mains (LV DC) to the PSU is sensed by the potential divider formed by R25, RN2C at R24 and is fed to the NI input pin 5 U1A. 5.1V reference is fed to the inverting pin 4 U1A and if the d.c. input falls to less than 16V – 17V the comparator output pin 2 U1A pulls down I LIM pin 1 of U6. This shuts down the PSU until the input d.c. rises back within specification. The PSU starts in its soft start mode.

Output Voltages from the Push-Pull Converter

The push pull converter produces the following outputs, some of which are used internally and some are outputted via three terminal regulators.

- +140V d.c. for internal use by PSU up converter producing HV for modulator.
- +50V d.c. for aerial turning motor.
- +16V d.c. magnetron heater circuit.
- ±12V, +5V for modulator and trigger board.
- +30V via up converter for tuning.
- +20V via up converter.

Zener diodes and resistors are connected across most outputs from the push-pull converter section to provide critical minimum current flow through the chokes to maintain the correct output voltage at all load conditions.

U7, U4, U2 are three terminal regulators which provide stabilisation and short circuit protection for the +5V ±12V rails.

The up converter takes the form of a flyback converter where the +140V rail generated by the push-pull converter is switched to the primary of transformer T2 by the power FET Q4. This FET is driven by the control circuitry within U5. Flyback action takes place during the off state. During the FET 'on ' state, energy is stored within the transformer T2. Switching aid networks comprising R44, C37, D27 and C38, D28, R38, R39, R40 serve to limit the flyback voltage appearing across Q4 during the transition period of on to off.

Primary current is sensed via R41 and is fed back to U5 via R60 with C39 filtering switching edges. This feedback provides overcurrent protection under fault conditions and stabilises the PSU under normal load conditions.

Initial start up voltage is provided from the +140V rail via R46 which charges C40 towards 17V. U5 starts when this voltage is achieved and then via voltage feedback action the p.w.m. chip U5 receives power from T2 via D35.

The flyback converter starts approximately 2 seconds after the push-pull converter has powered up due to the charging action of C40 via R46. Should an output over-current fault occur then the up-converter hiccups on/off with approximately 1 second repetition rate until the fault has been rectified.

Voltage feedback also occurs via T2 winding, D35 and potential divider formed by R48, R49, R54 and RV1. Rv1 sets the voltage at pin 2 U5 and adjusts the HV output over the range 550V to 650V. Thus the magnetron anode current is adjusted via the modulator. To produce the –600V d.c. HT, three windings on the secondary of T2 each produce 200V and are added together at the output of the rectifier circuits.The 30V circuit is fed via a three terminal regulator used to absorb the varying output of T2 when RV1 is adjusted for various settings of the HT. The 20V rail is stabilised using D22 from the 30V output.

The flyback converter operates at approximately 40kHz.

The motor (aerial supply) is approximately 50V with a starting current capability of up to 5A. The usual running current is from 1-2A. Zener diode D47, together with R67 provide enough critical current load to prevent the output voltage rising above 60V under very light or no load conditions.

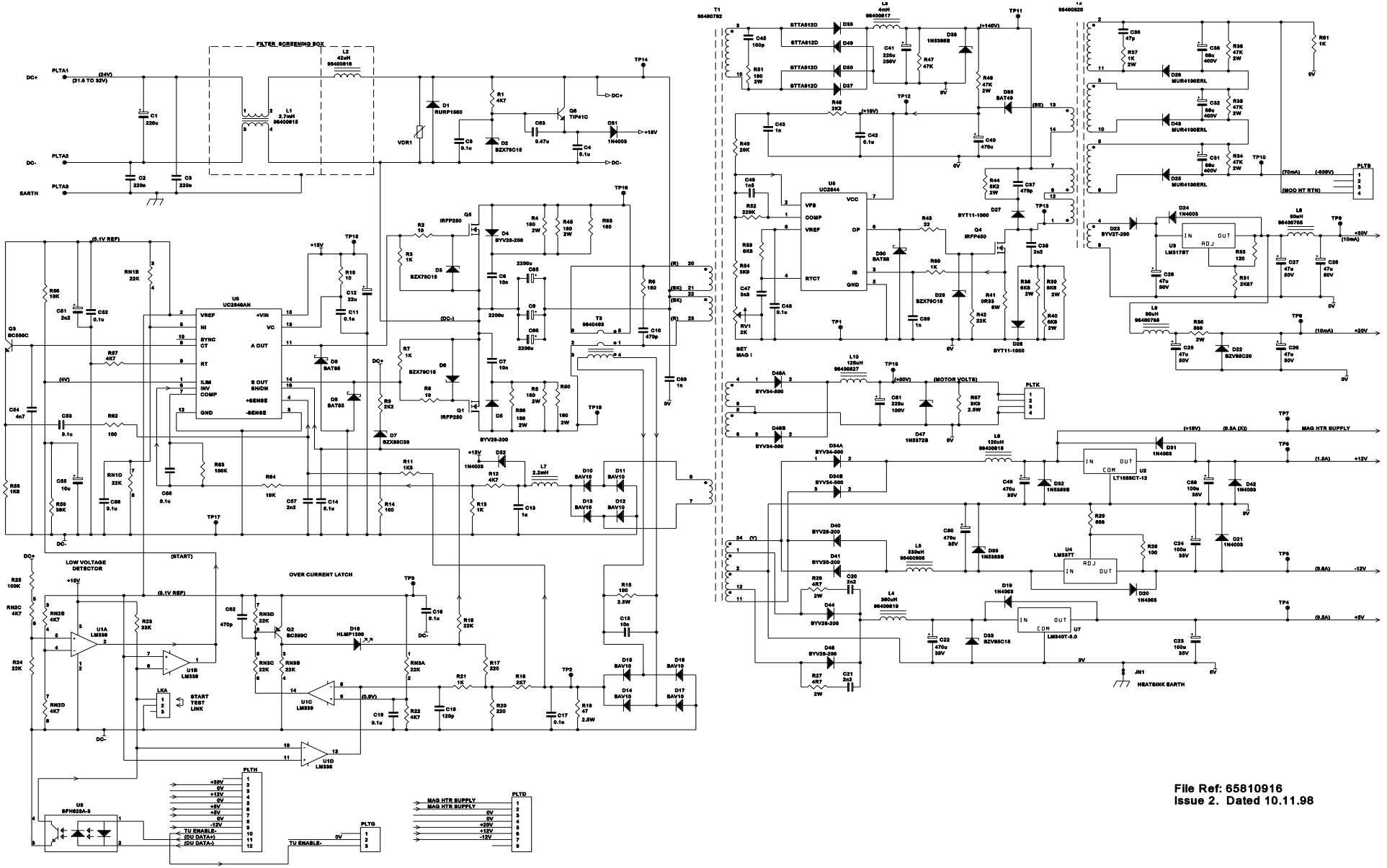

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Figure 2.35 X-Band Transceiver DC Power Supply Board

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