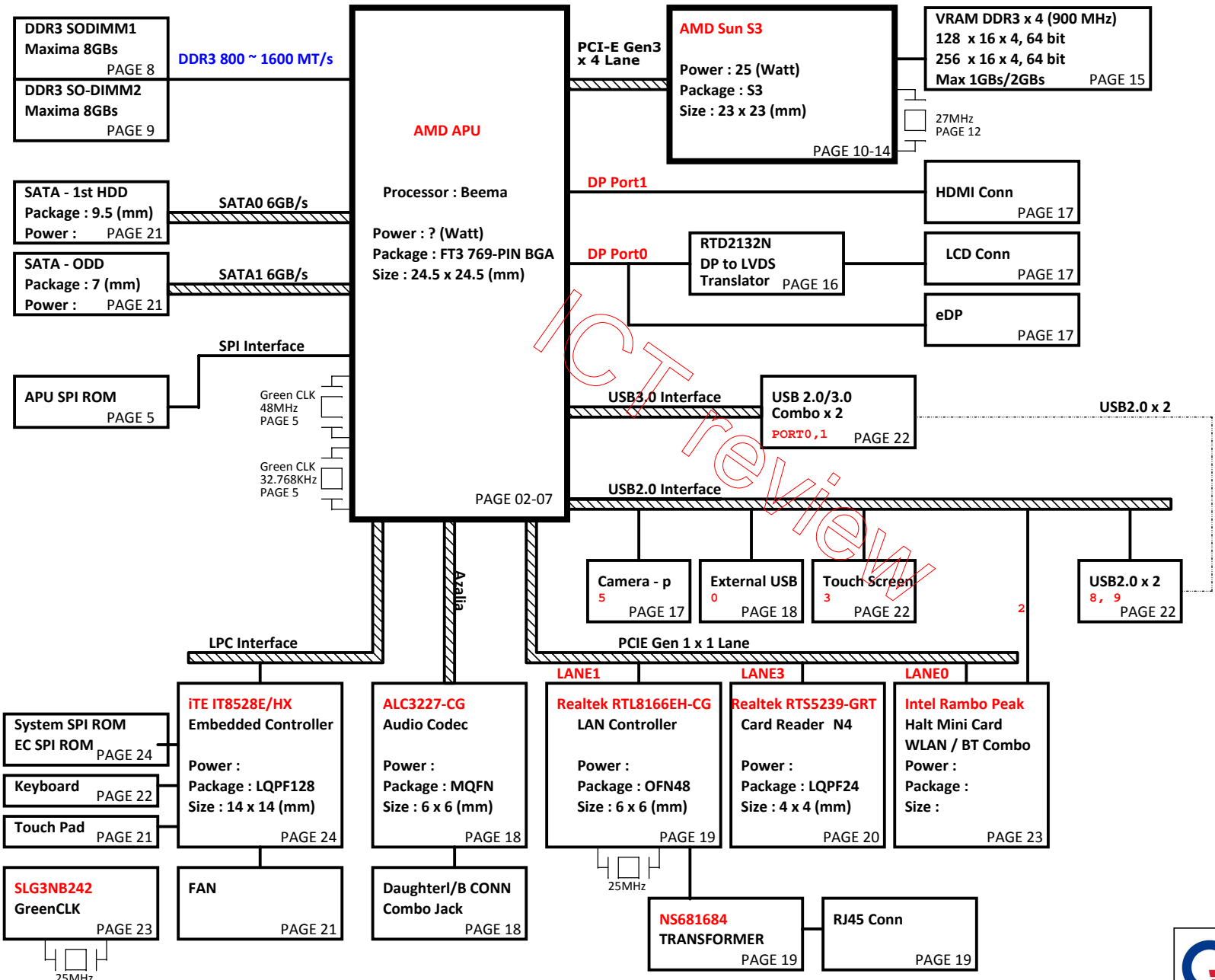


Lean G_AMD Beema DIS/UMA (14"/15.6")

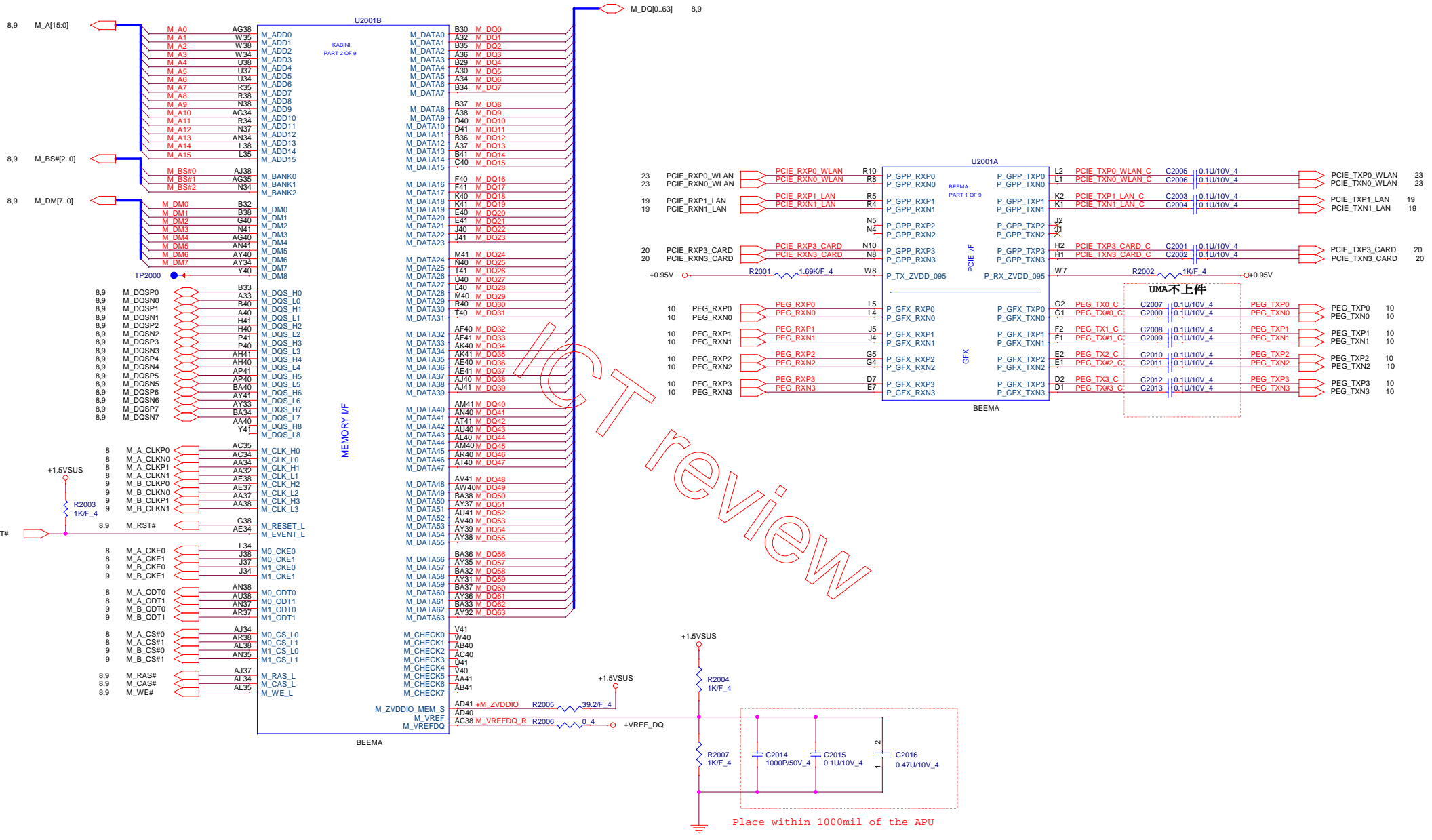
Ultra/Slim



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

- Power Source**
- TI BQ24728**
System Charge Power (+BATCHG)
PAGE 25
 - Ricteck RT8223PZ**
System Power (+3VPCU/+5VPCU/
+3VSS/+5VSS)
PAGE 26
 - AOZ1237QI/APW8824CTI/G9183**
KABINI Power (+0.95V/+0.95VSS
/+1.5VSS)
PAGE 27
 - TI TPS51216**
System Memory Power (+1.5VSSUS/
+0.75V_DDR_VTT)
Ricteck RT8068A
KABINI Power (+1.8VSS)
PAGE 28
 - Intersil ISL6277HRTZ/ISL6208BCRZ**
Processor Power (+VCC_CORE/
+VDDNB_CORE)
PAGE 29~30
 - GMT G5934RZ1U**
System Discharge Power
(+1.5V/+3V/+5V)
(+3VSSUS/+3VLANVCC/+1.8V)
PAGE 31
 - On-semi ADP3211A**
VGA Power (+VGA_CORE)
PAGE 32
 - Ricteck RT8086A**
DGPU Power (+1.0V_VGA/+3V_VGA
/+1.5V_VGA/+1.8V_VGA/)
PAGE 33

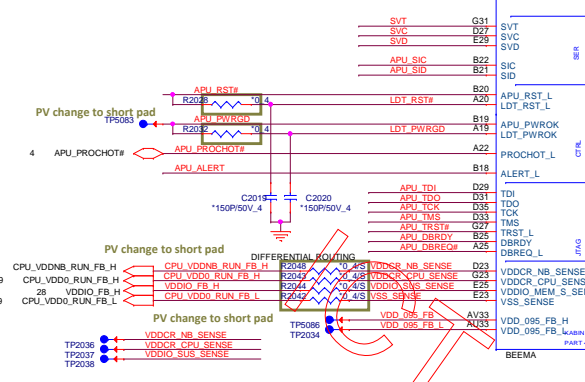
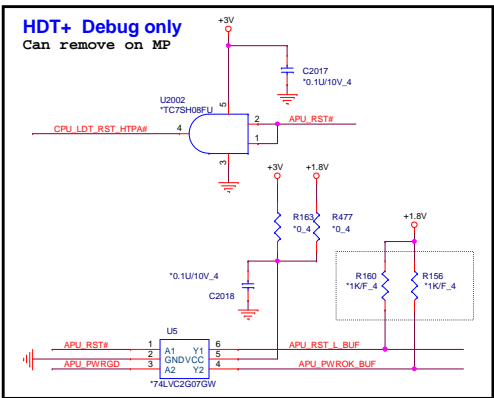
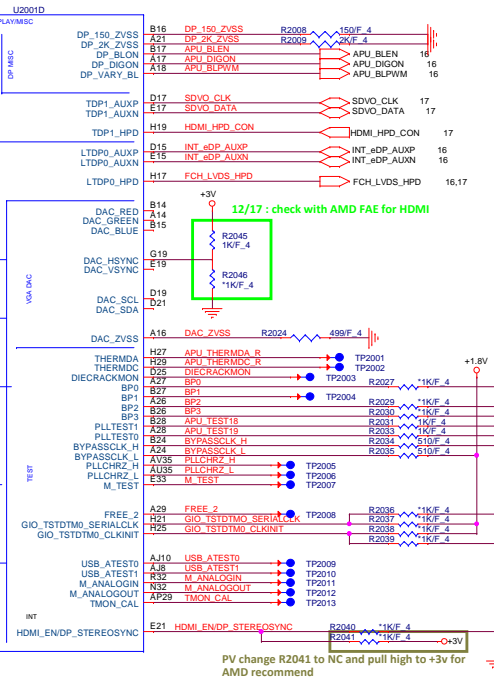
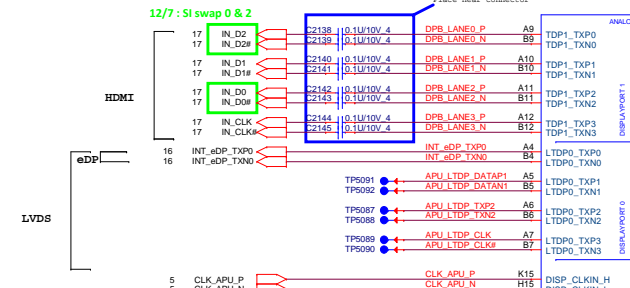
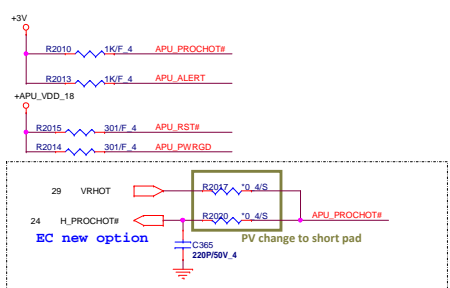


IC T review

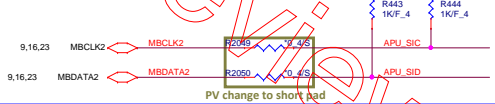
Place within 1000mil of the APU

6,8,9,28,31,33	+1.5VSUS	
8,9	+VREF_DQ	
5,6,27	+0.95V	

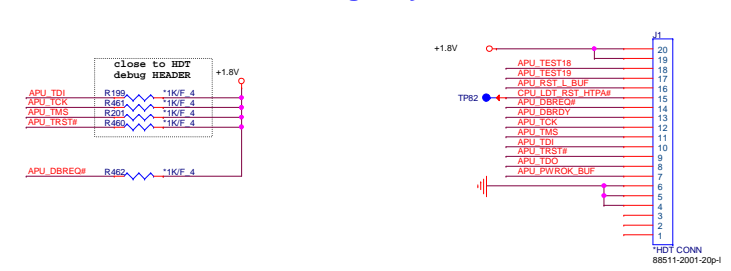
	INT PROJECT :U99 Quanta Computer Inc.		Rev 1A
	Size Document Number MEM/PCIE (1/6)	Date: Monday, May 19, 2014 Sheet 2 of 33	



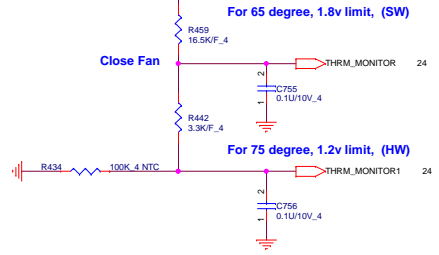
Thermal Sensor



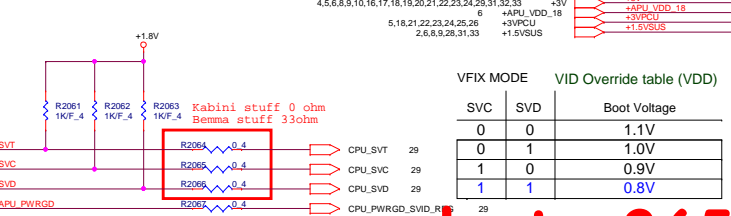
HDT+ Connector for Debug only



IO Thrm Protect

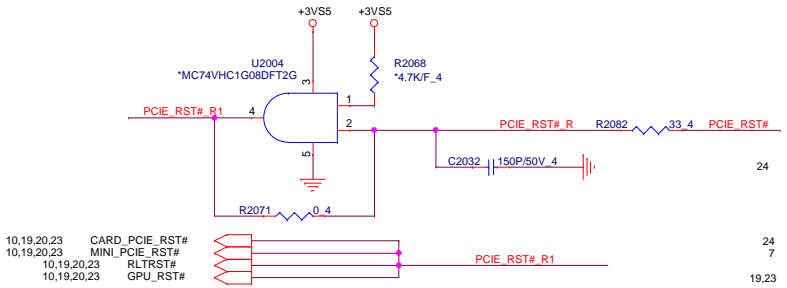


Serial VID

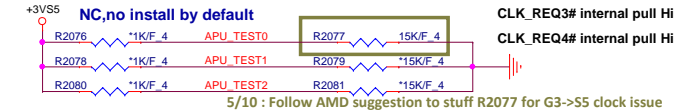
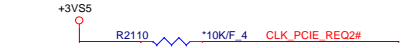


VFIX MODE VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

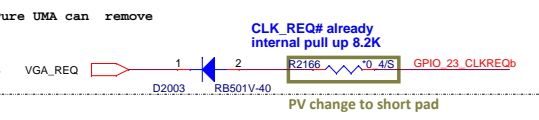
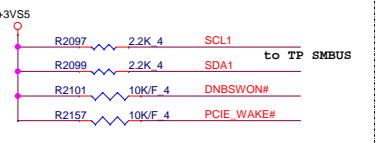
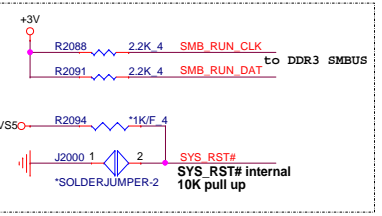


10,19,20,23 CARD_PCIE_RST#
 10,19,20,23 MINI_PCIE_RST#
 10,19,20,23 RLTRST#
 10,19,20,23 GPU_RST#



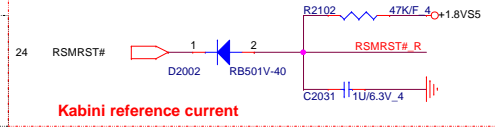
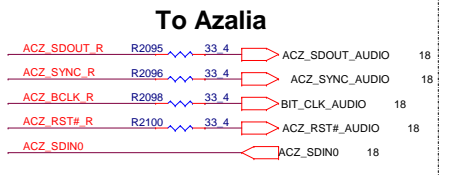
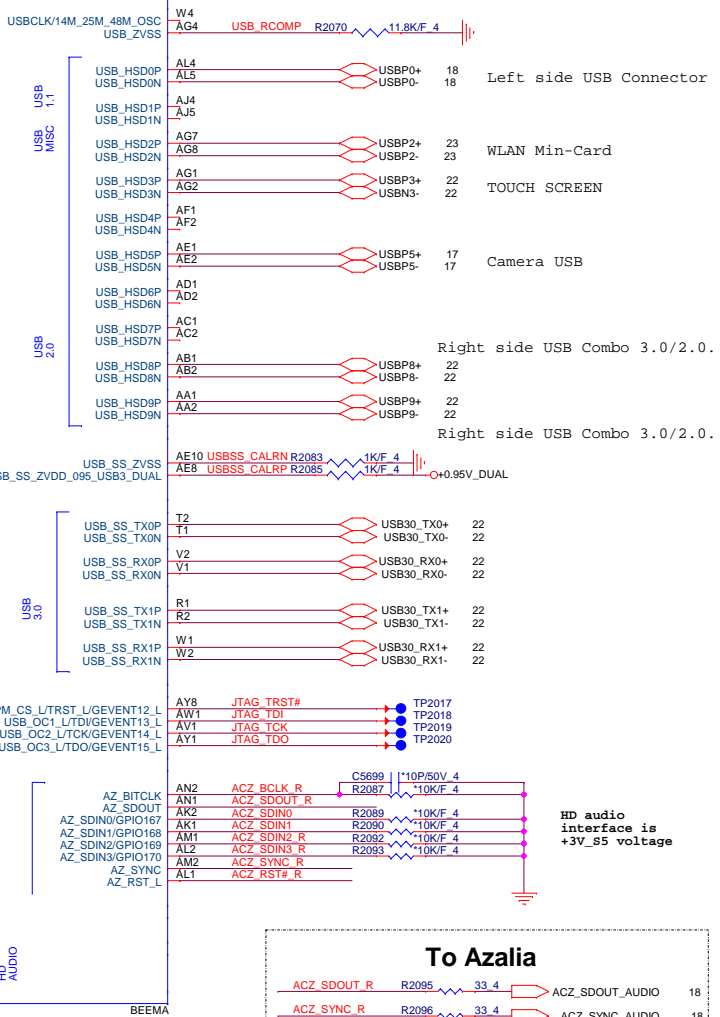
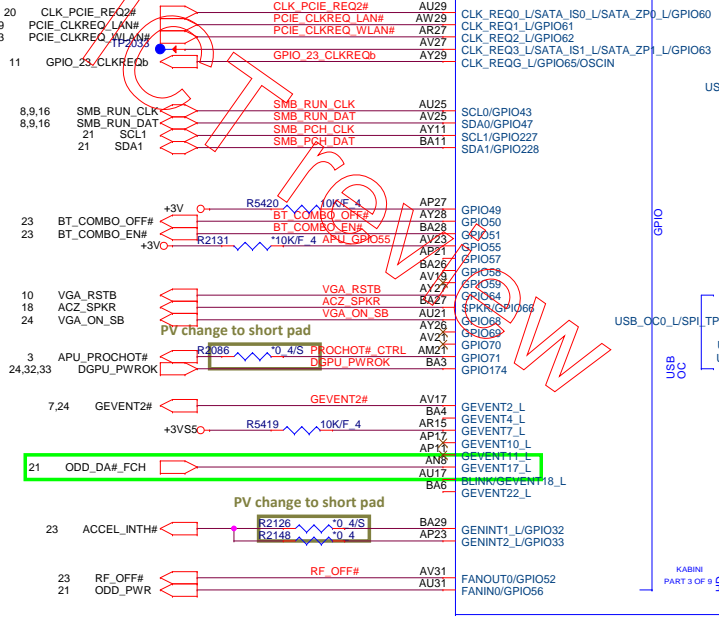
5/10 : Follow AMD suggestion to stuff R2077 for G3->S5 clock issue

TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted. FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins.
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins.
1	TMS	1	Use on ATE only Yuba JTAG enabled



CLK_REQ2# internal pull Hi 8.2K to +3V
 CLK_REQ3# internal pull Hi 8.2K to +3V
 CLK_REQ4# internal pull Hi 8.2K to +3V

3/4 : Follow BIOS suggestion change ODD detect to GEVENT



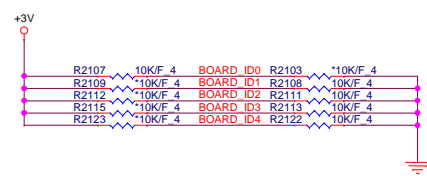
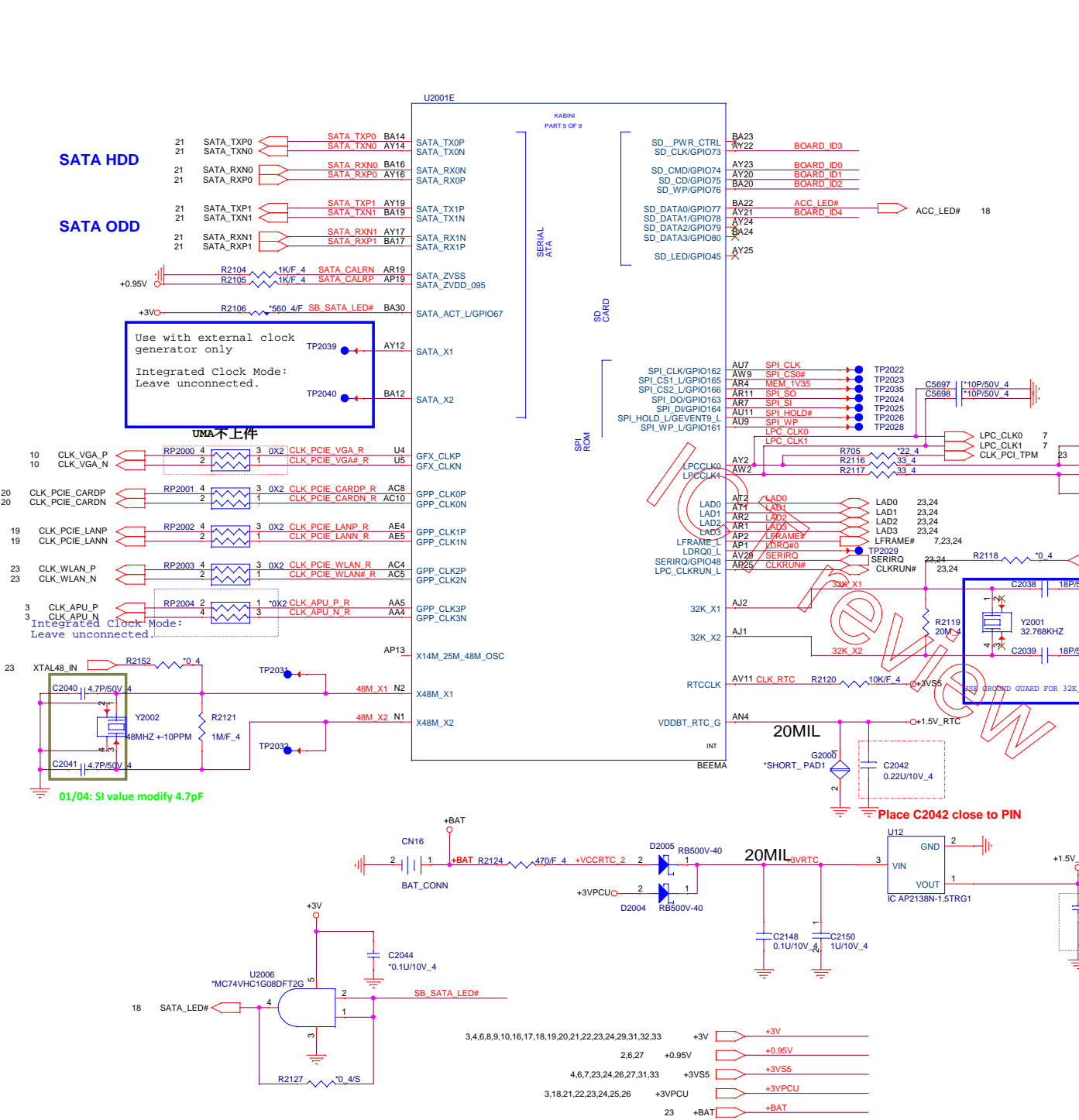
Kabini reference current



PROJECT :U99
 Quanta Computer Inc.

Size: Document Number: **GPIO/USB/AZ (3/6)** Rev: 1A

Date: Monday, May 19, 2014 Sheet: 4 of 33



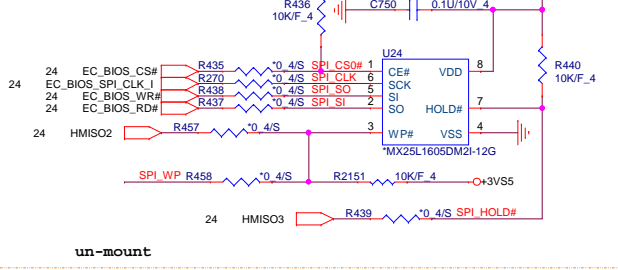
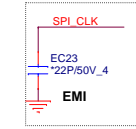
BOARD ID SETTING

Model	BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	BOARD_ID4
14" UMA	0	0	0	0	0
15" UMA	0	1	0	0	0
14" DIS	1	0	0	0	0
15" DIS	1	1	0	0	0

APU SPI ROM

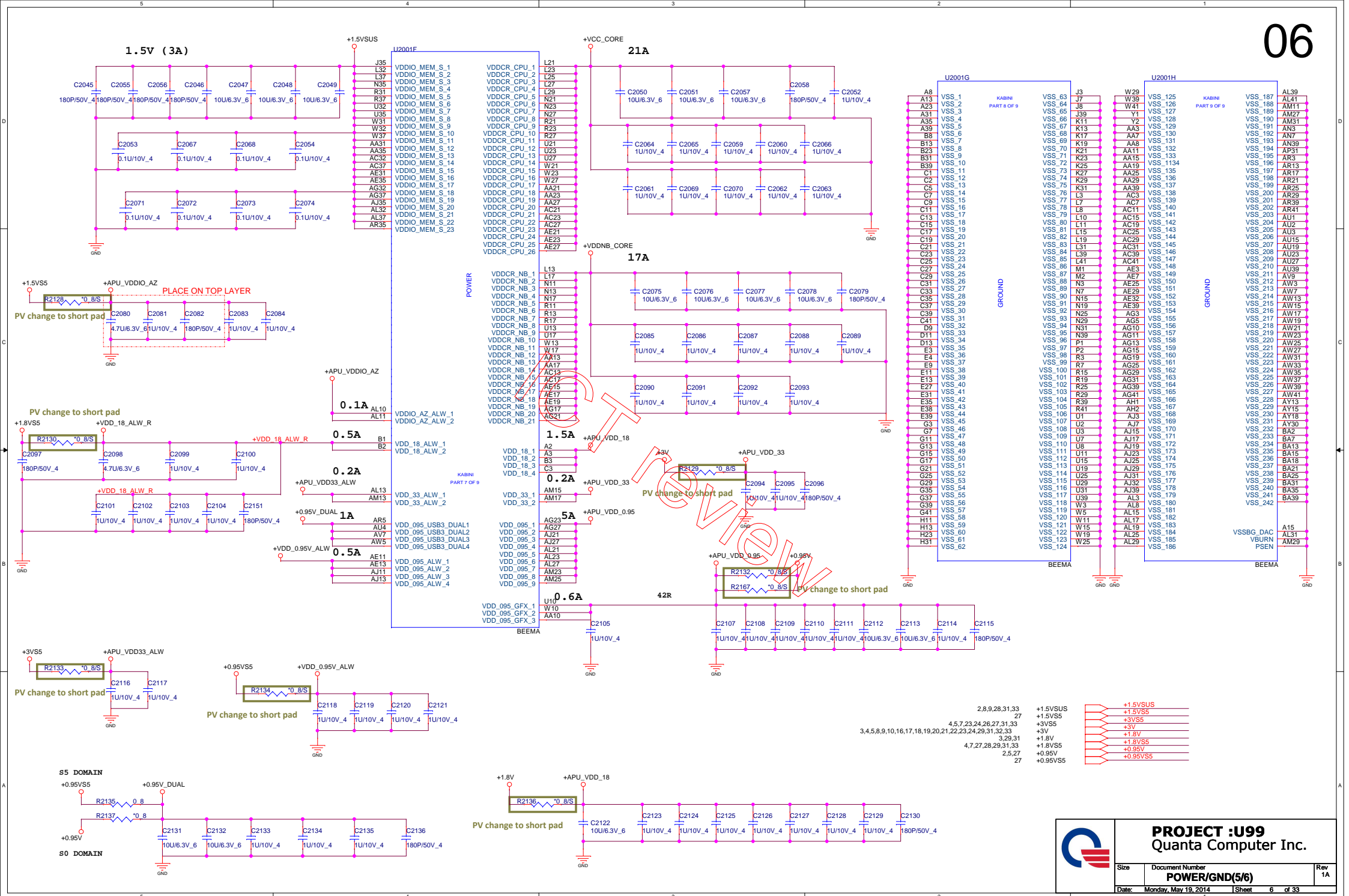
Replace to MX25L6436E

Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023



PROJECT :U99
Quanta Computer Inc.

Size	Document Number	Rev
	SATA/CLK (4/6)	1A
Date:	Monday, May 19, 2014	Sheet 5 of 33



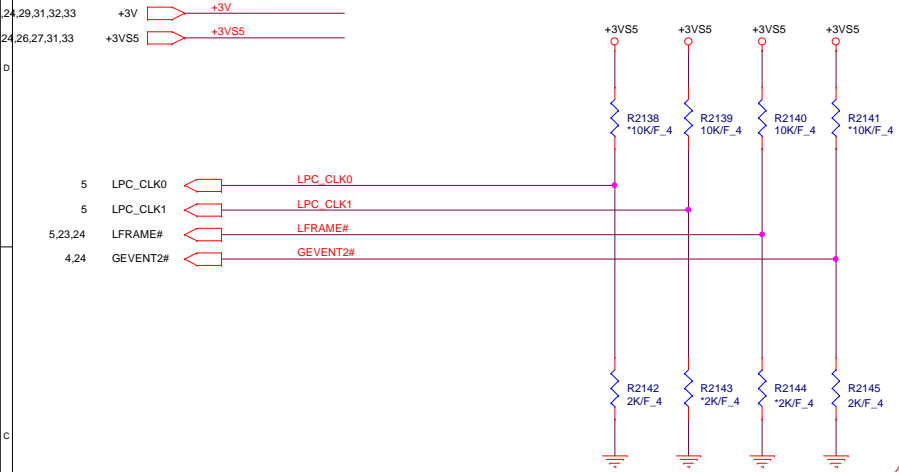
Legend table listing voltage levels (e.g., +1.5VSUS, +1.5VSS, +3VS5, +3V, +1.8V, +1.8VSS, +0.95V, +0.95VS5) and corresponding color-coded lines used in the schematic.

PROJECT :U99 Quanta Computer Inc.
Size Document Number: POWER/GND(5/6) Rev 1A
Date: Monday, May 19, 2014 Sheet 6 of 33

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS

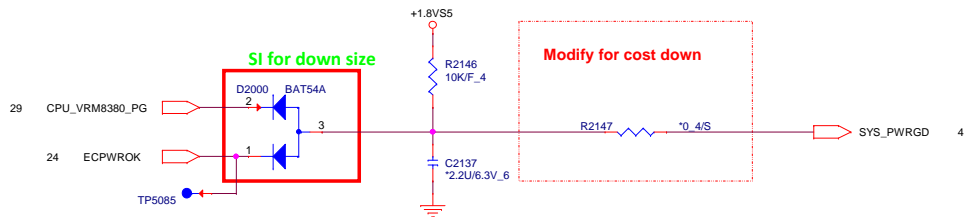


REQUIRED STRAPS

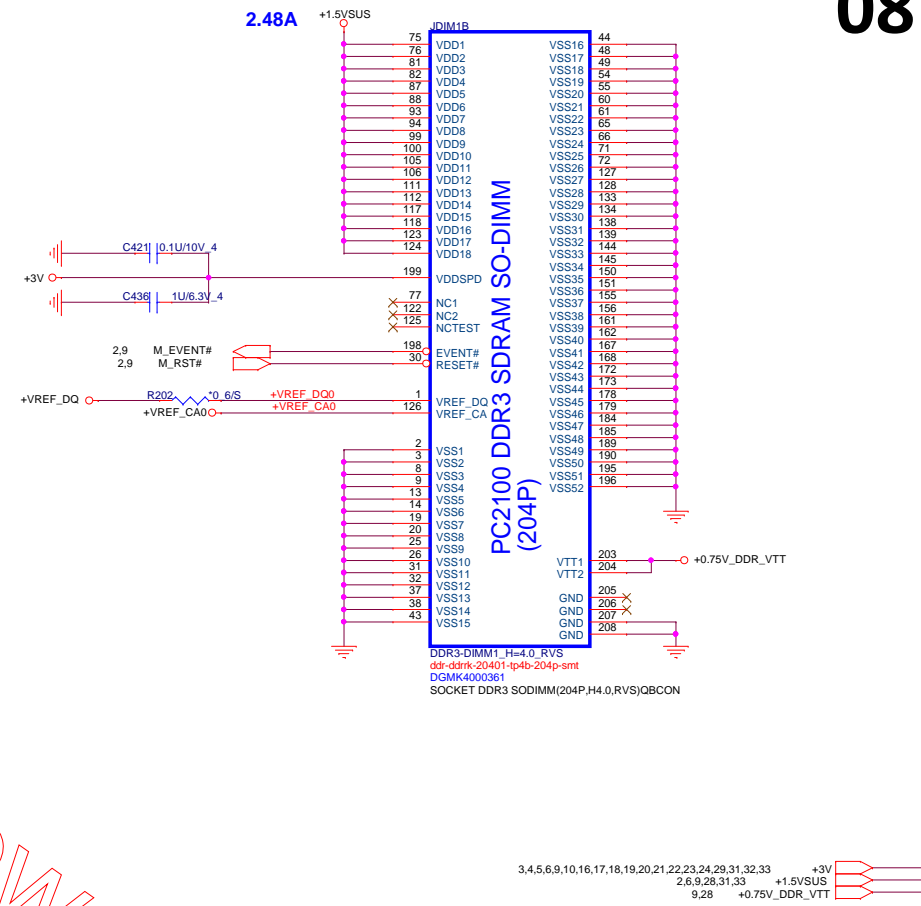
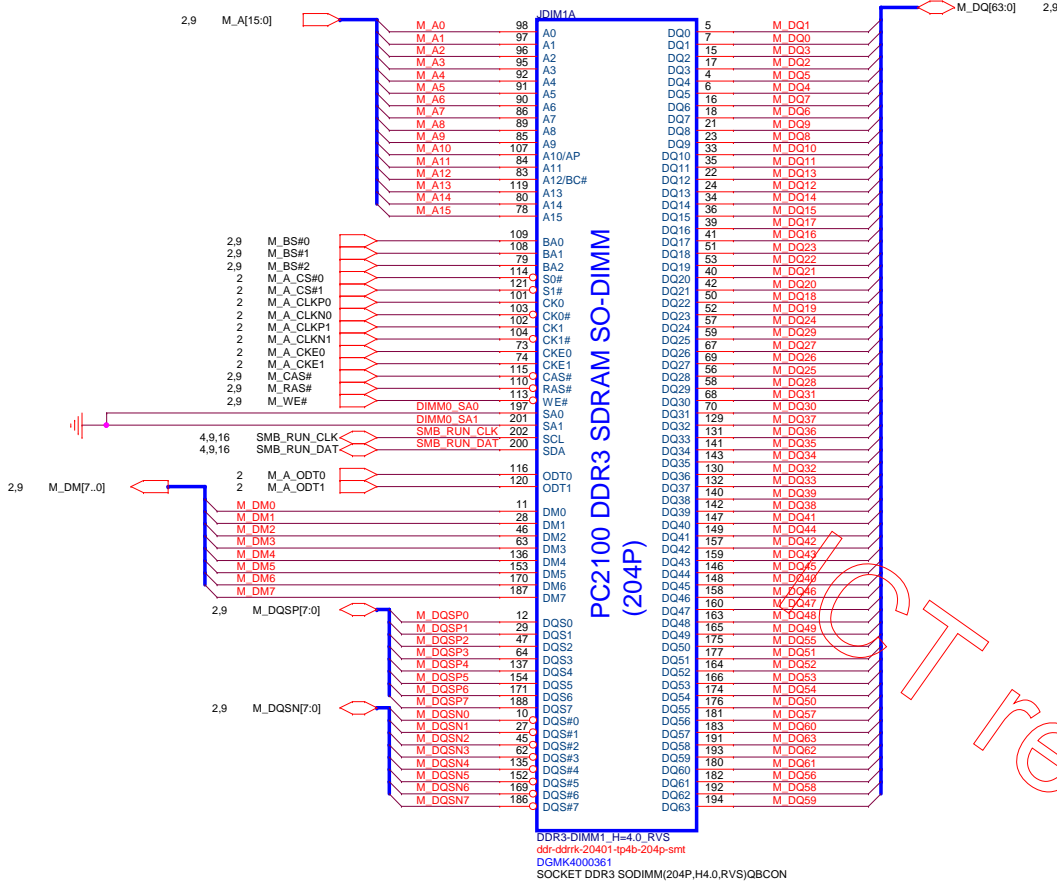
				LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH				BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW				BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT

ICM review

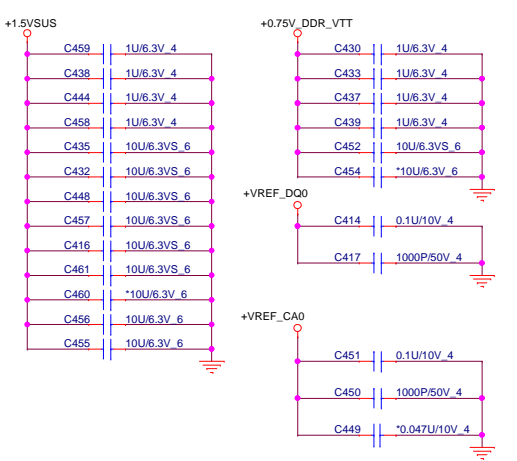
SYS PWGRD



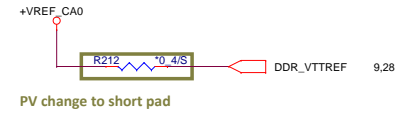
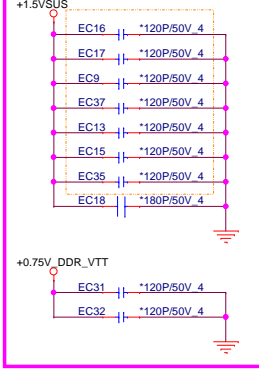
	PROJECT :U99 Quanta Computer Inc.		
	Size	Document Number	Rev
		STRAP (6/6)	1A
Date: Monday, May 19, 2014 Sheet 7 of 33			



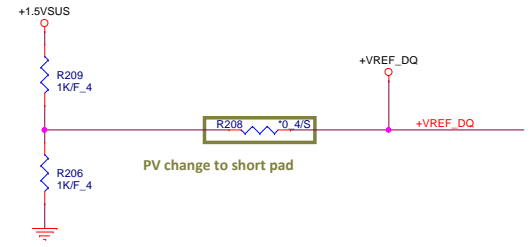
Place these Caps near So-Dimm0.



For EMI RESERVE

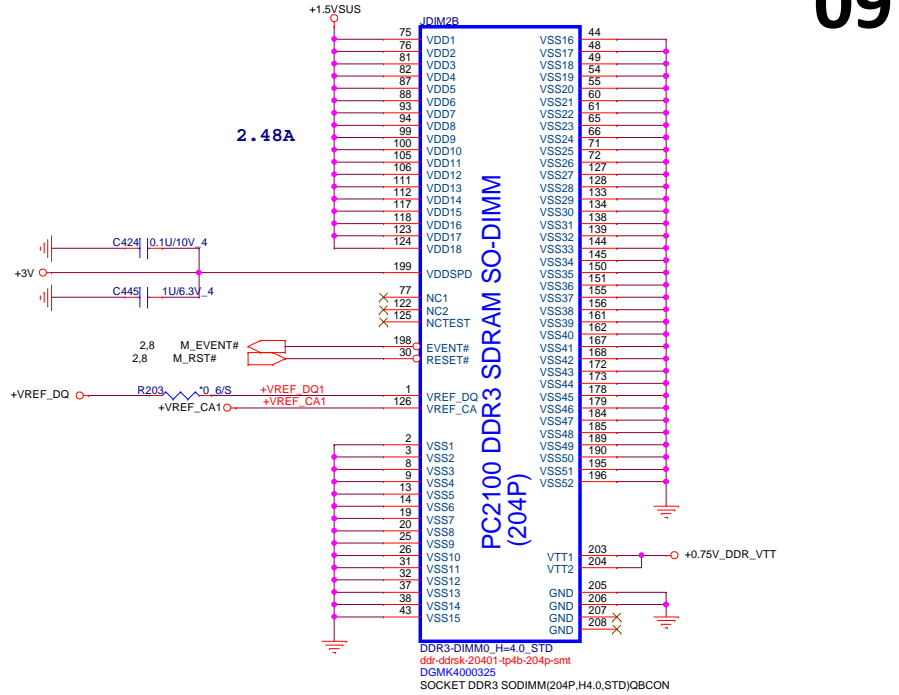
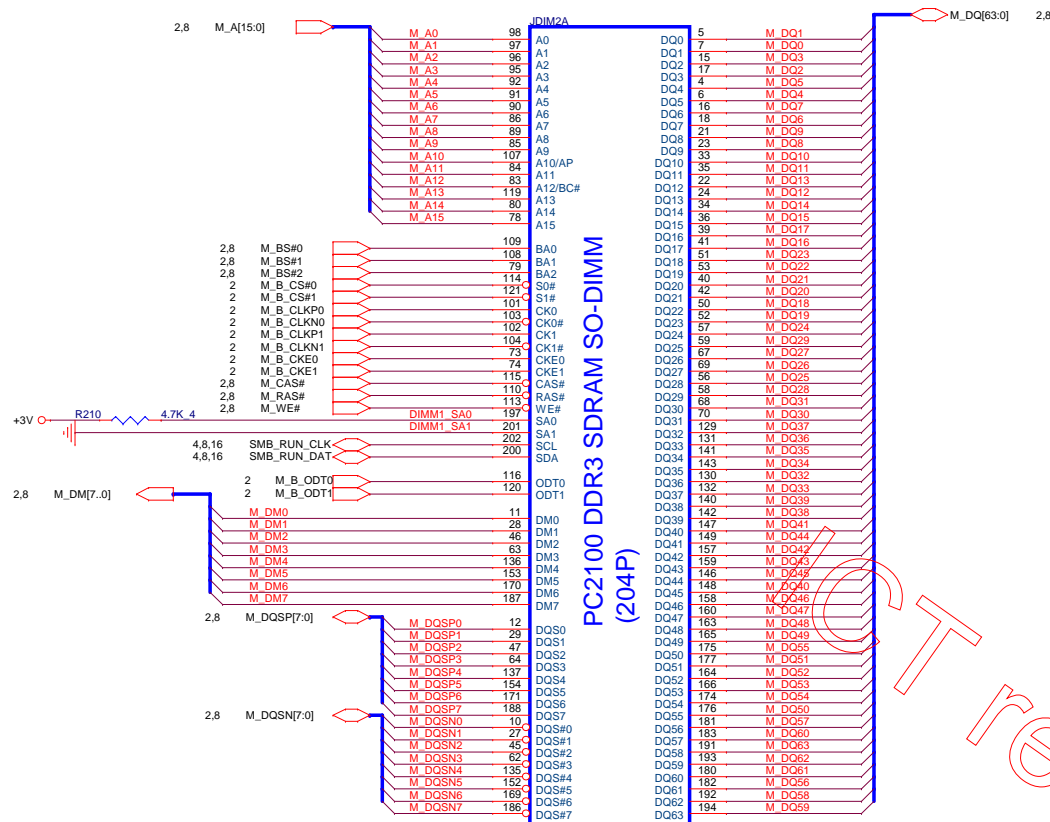


Reserved for AMD suggest



PROJECT :U99
 Quanta Computer Inc.

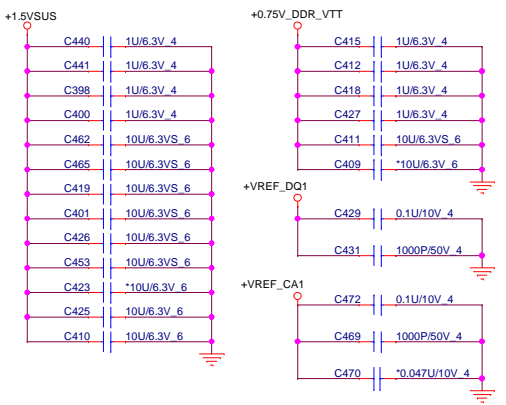
Size Custom	Document Number System Memory 1/2 (5.2H)	Rev 1A
Date: Monday, May 19, 2014	Sheet 8 of 33	



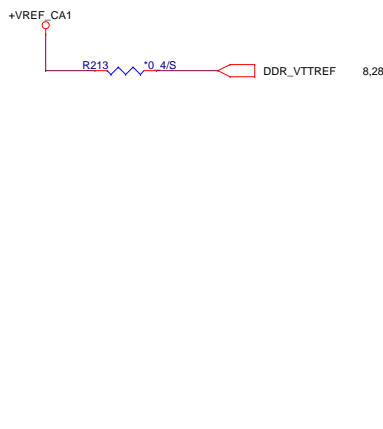
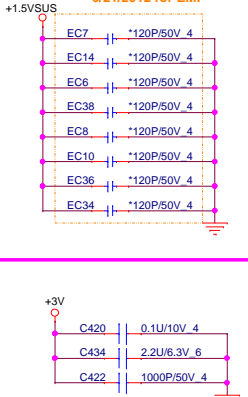
DDR3-DIMM0_H=4.0_STD
 ddr-ddrsk-20401-tp4b-204p-smt
 DGMK4000325
 SOCKET DDR3 SODIMM(204P,H4.0,STD)QBCCN

3.4,5,6,8,10,16,17,18,19,20,21,22,23,24,29,31,32,33 +3V
 2.6,8,28,31,33 +1.5VSUS
 8,28 +0.75V_DDR_VTT

Place these Caps near So-Dimm1.

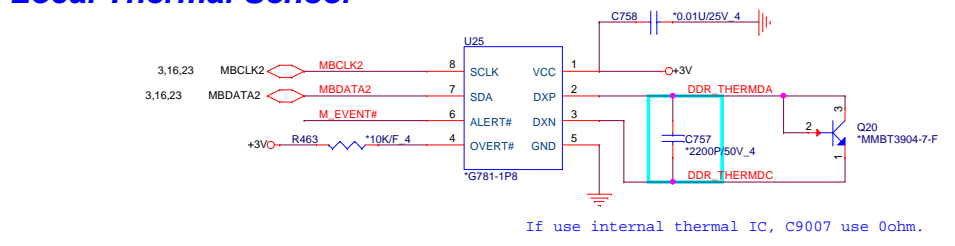


For EMI RESERVE
 6/21/2012 for EMI



Local Thermal Sensor

DDR3 Thermal Sensor

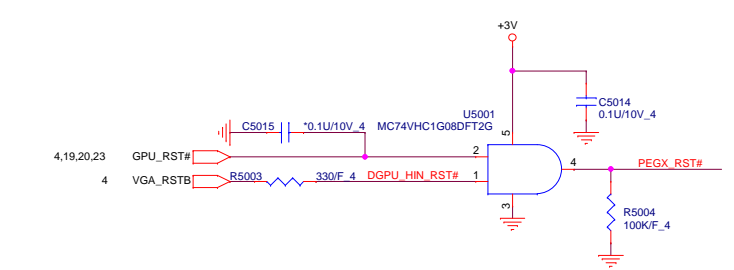
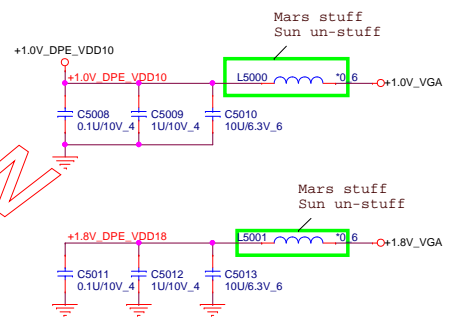
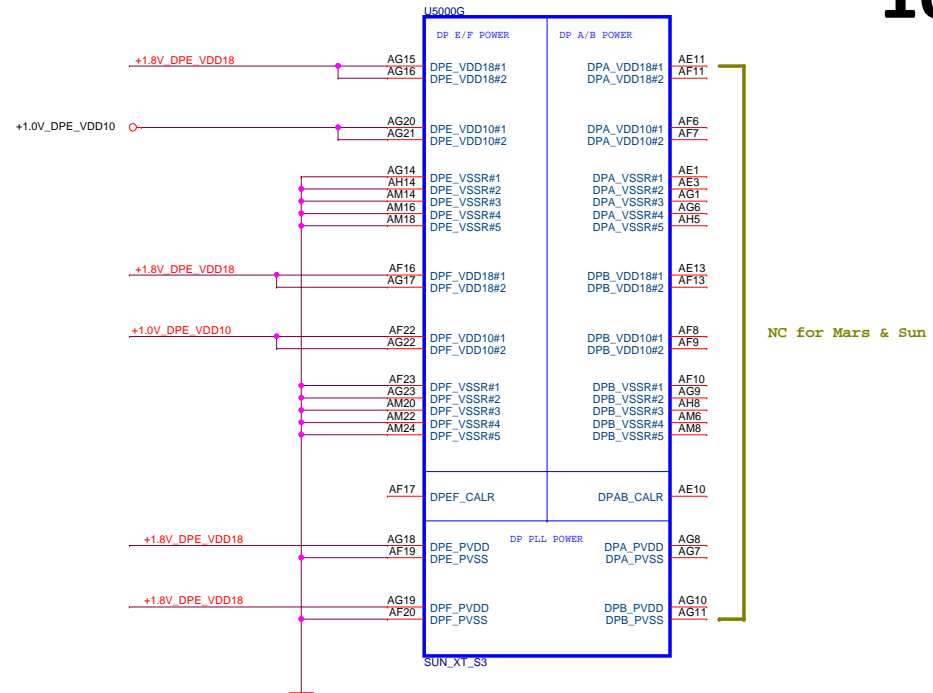
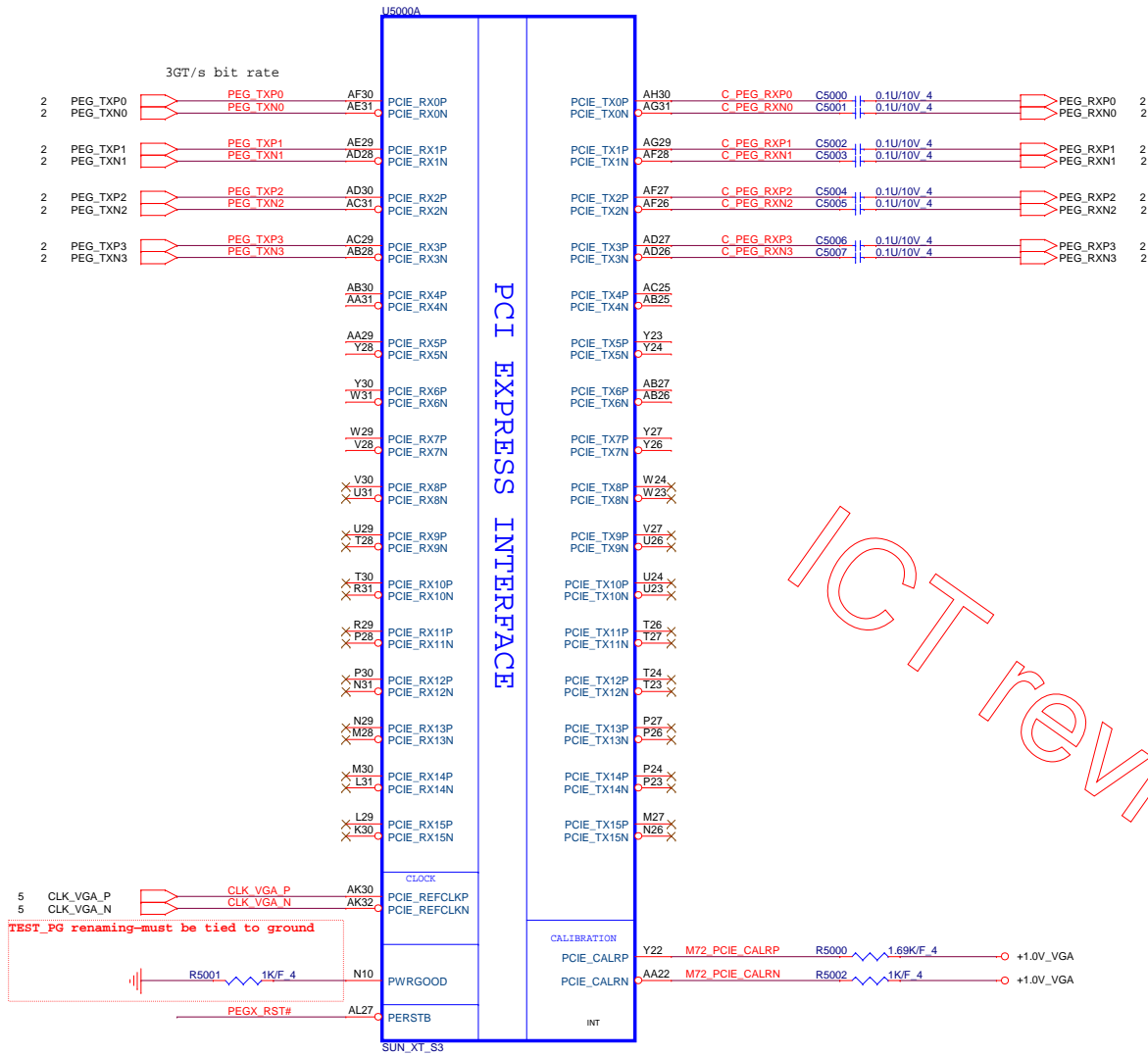


Main:AL000781039 G781-1P8(9Ah)
 2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Main:AL001412003 EMC1412-1-ACZL-TR(98h)
 2nd:AL000431014 TMP431ADGKR(98h)

PROJECT :U99
Quanta Computer Inc.

Size Custom	Document Number System Memory 2/2 (9.2H)	Rev 1A
Date: Monday, May 19, 2014	Sheet 9 of 33	



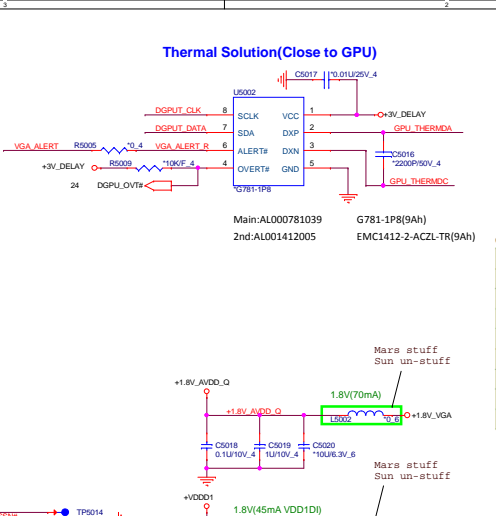
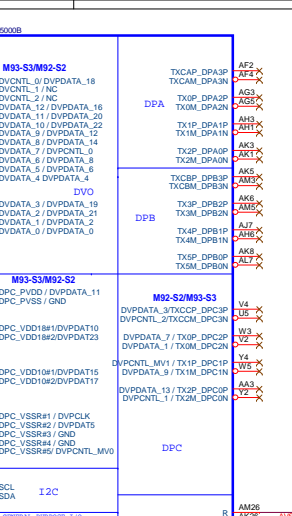
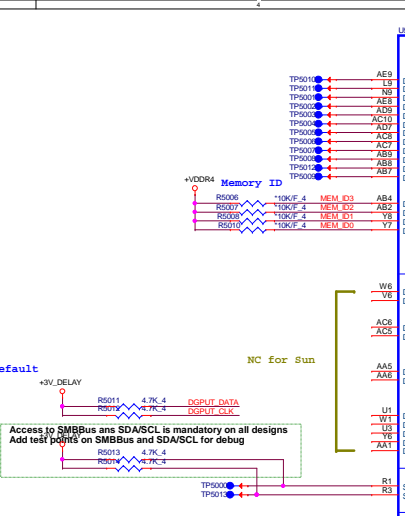
ICT review

NC for Mars & Sun

PROJECT :U99
Quanta Computer Inc.

Size Custom	Document Number Sun S3 PCIe Interface	Rev 1A
Date: Monday, May 19, 2014 Sheet 10 of 33		

GPIO10	GPIO30	GPIO6	GPIO12	GPIO20	GPIO15	Sun XT 33
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE	
0	1	1	0	1	1.175V	
0	1	1	1	0	1.150V	
0	1	1	1	1	1.125V	
1	0	0	0	0	1.100V	
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	
1	1	1	0	1	0.775V	

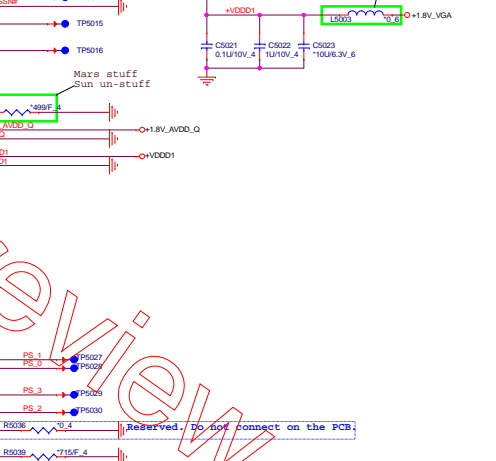
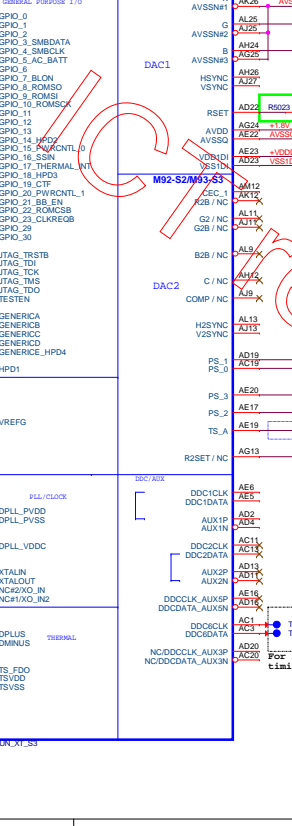
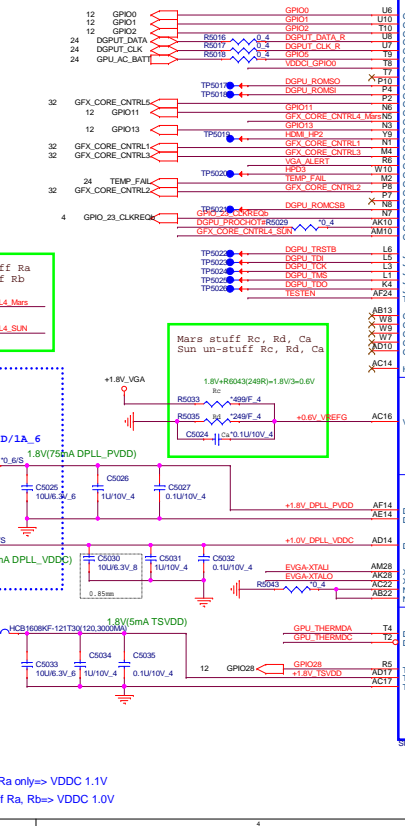
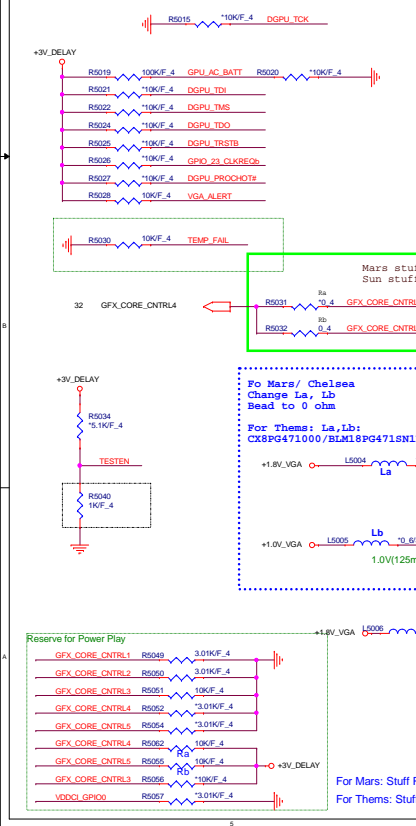


MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0, 1, 2 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Place PS circuit components as close to PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

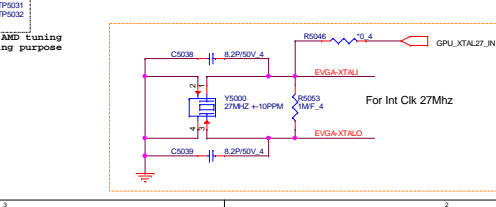
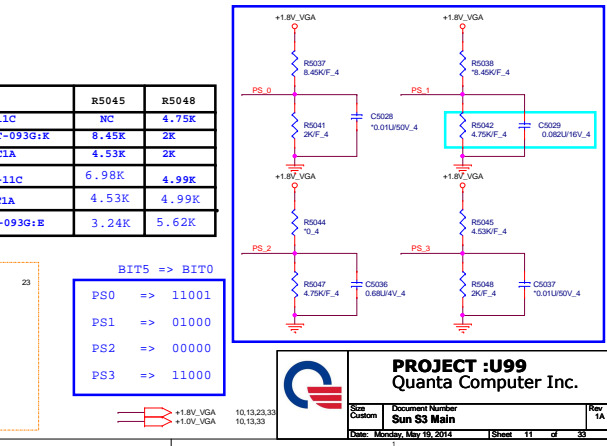
C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111



Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidfg[2:0] define memory aperture size. If bios_rom_en = 1, romidfg[2:0] define ROM type	xxx	gpio_13, gpio_12, gpio_11
PS_0[4]	n/a	Reserved	1	genk_vsync
PS_1[1]	bf_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bf_clk_pm_en	PCIe CLK PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genk_clk
PS_1[4]	tx_pwrsv_erb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_cp[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_cp[1]			
PS_0[5]	aud_port_cp[0]			

PS_3[3:1]	Vendor	Type	Vendor P/N	R5045	R5048
000	Hynix - F(Huma)	128Mx16 *4, 900Mhz	H57C2G63PFR-11C	NC	4.75K
001	Micron - V89C/E	128Mx16 *4, 900Mhz	MT41J128M16J7-093G:E	8.45K	2K
010	Samsung- B die	128Mx16 *4, 900Mhz	K4W2G1646B-BCLIA	4.53K	2K
011	Hynix - Huma die	256Mx16 *4, 900Mhz	H57C4G63PFR-11C	6.98K	4.99K
100	Samsung- B die	256Mx16 *4, 900Mhz	K4W4G1646B-HCLIA	4.53K	4.99K
101	Micron - E	256Mx16 *4, 900Mhz	MT41J256M16HA-093G:E	3.24K	5.62K



BIT5 => BIT0

PS0 => 11001

PS1 => 01000

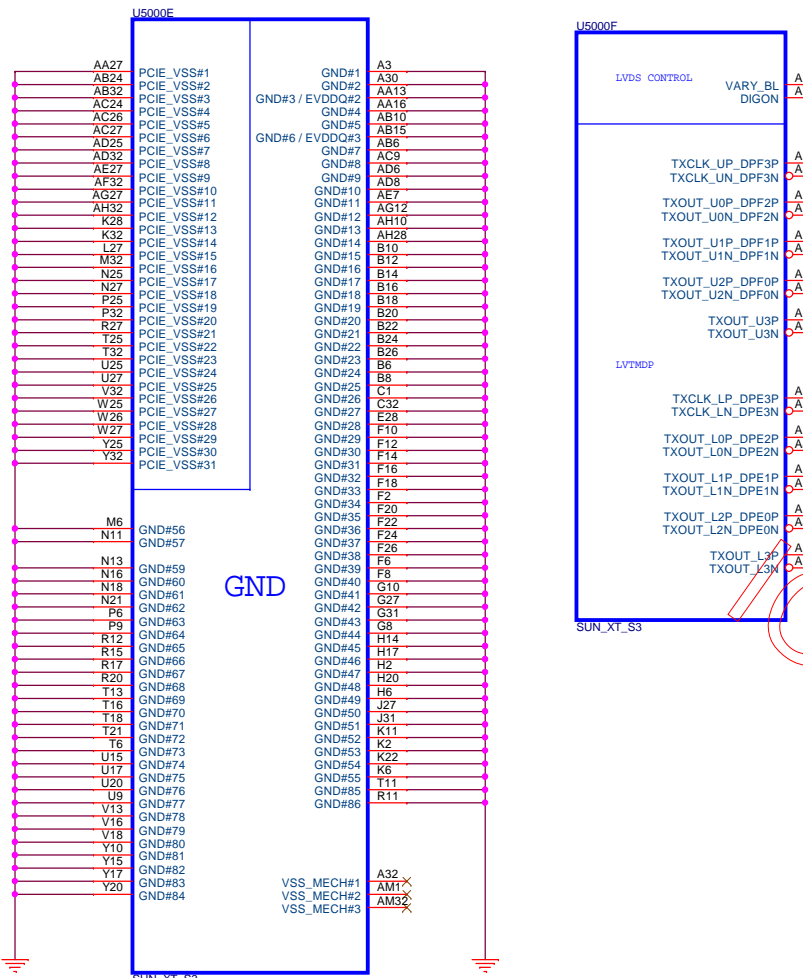
PS2 => 00000

PS3 => 11000

PROJECT :U99
Quanta Computer Inc.

Doc Custom Document Number: Sun S3 Main Rev 1A

Date: Monday, May 19, 2014 10.13.23.33 10.13.33 Sheet 11 of 33



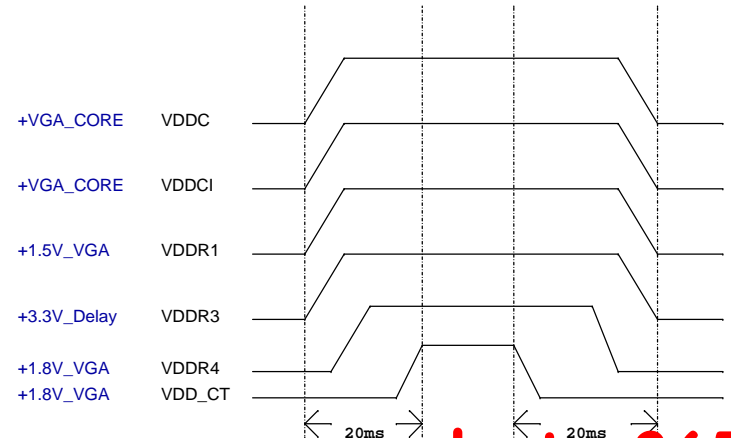
CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
RSVD	GPIO2	RESERVED	X
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

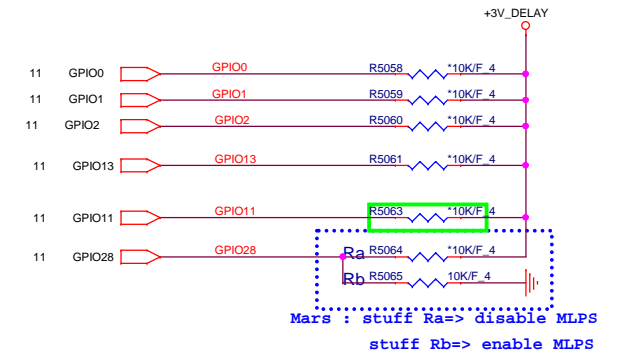
GPIO21	H2SYNC	GENERICC	GPIO8	GPIO2
--------	--------	----------	-------	-------

Power Up/Down Sequence



Memory Aperture size(Seymour)

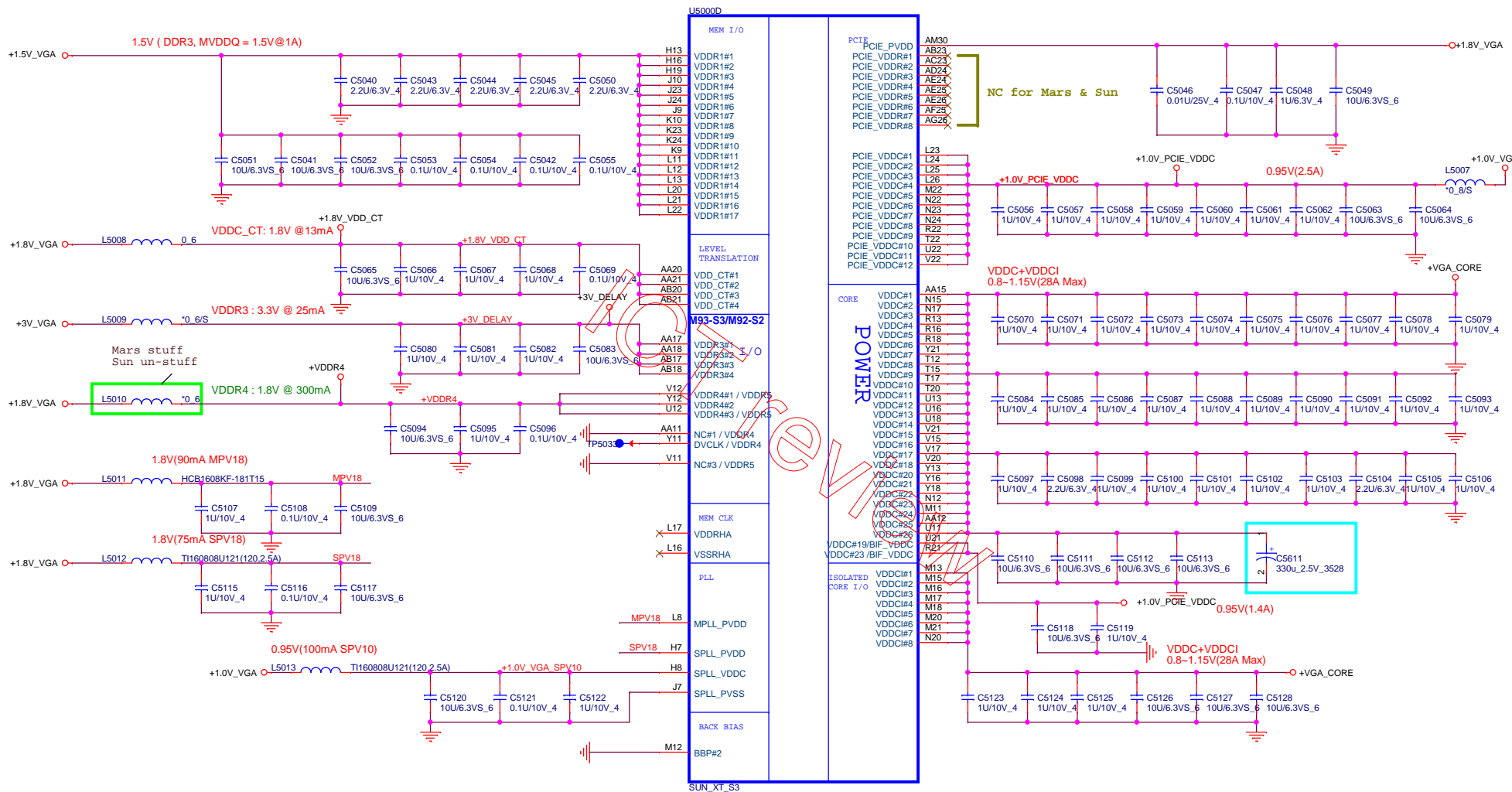
GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	0
0	32M	0	1
0	512M	1	0
0	1G	1	1
0	2G	1	0
0	4G	1	1



It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

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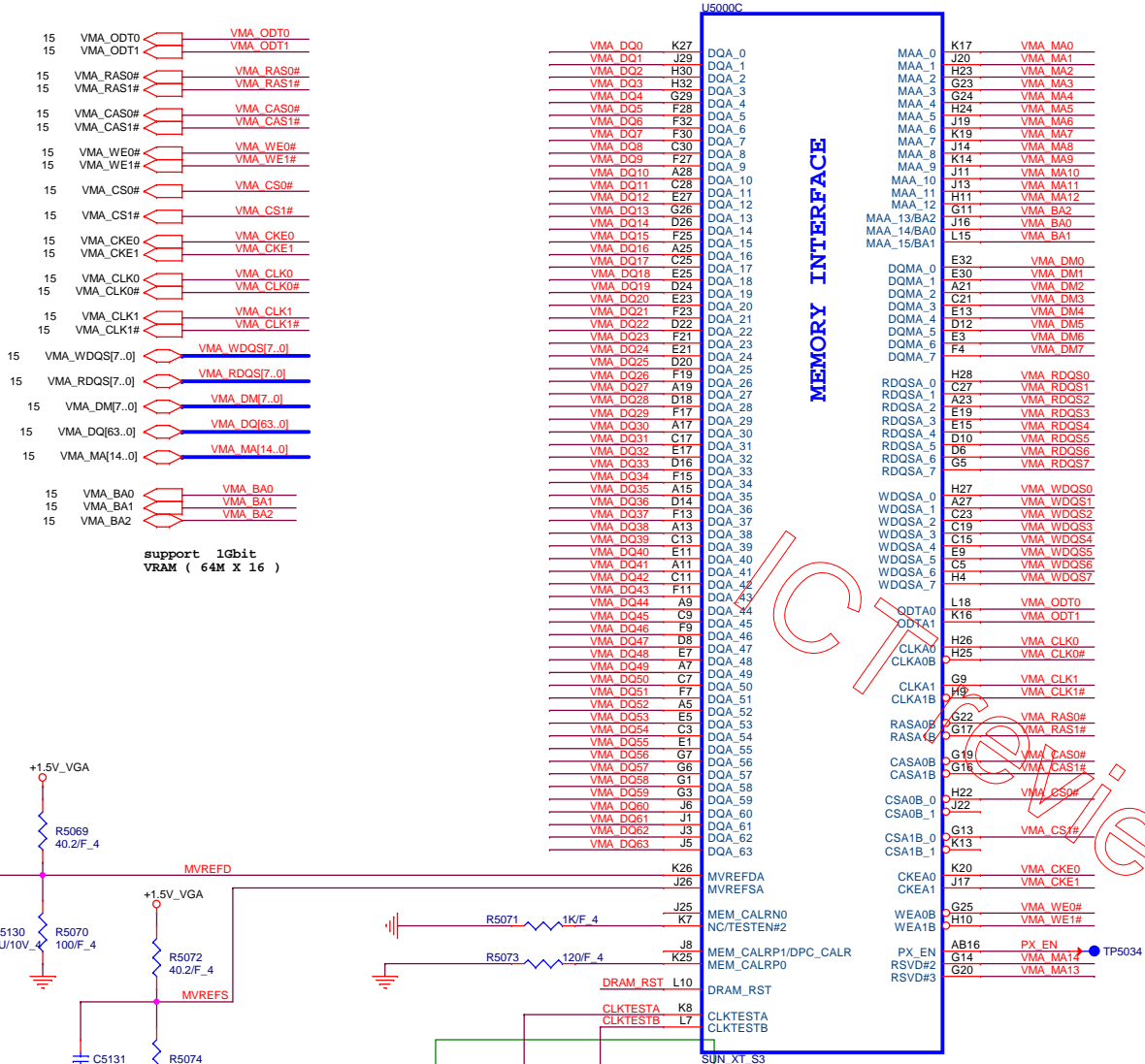
Size Custom	Document Number Sun S3 GND / LVDS/ Straps	Rev 1A
Date: Monday, May 19, 2014	Sheet 12 of 33	



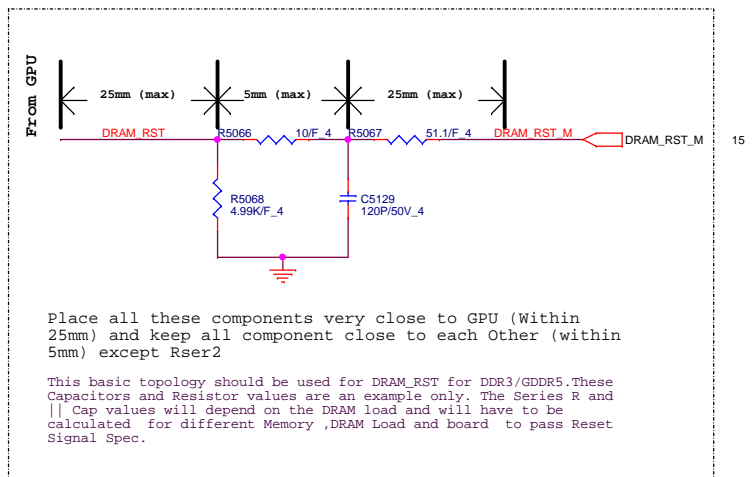
+1.5V_VGA	14,15,33
+1.8V_VGA	10,11,23,33
+1.0V_VGA	10,11,33
+VGA_CORE	32,33
+3V	3,4,5,6,8,9,10,16,17,18,19,20,21,22,23,24,29,31,32,33
+5V	17,18,21,22,31

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Size Custom	Document Number Sun S3 Power_and_NC	Rev 1A
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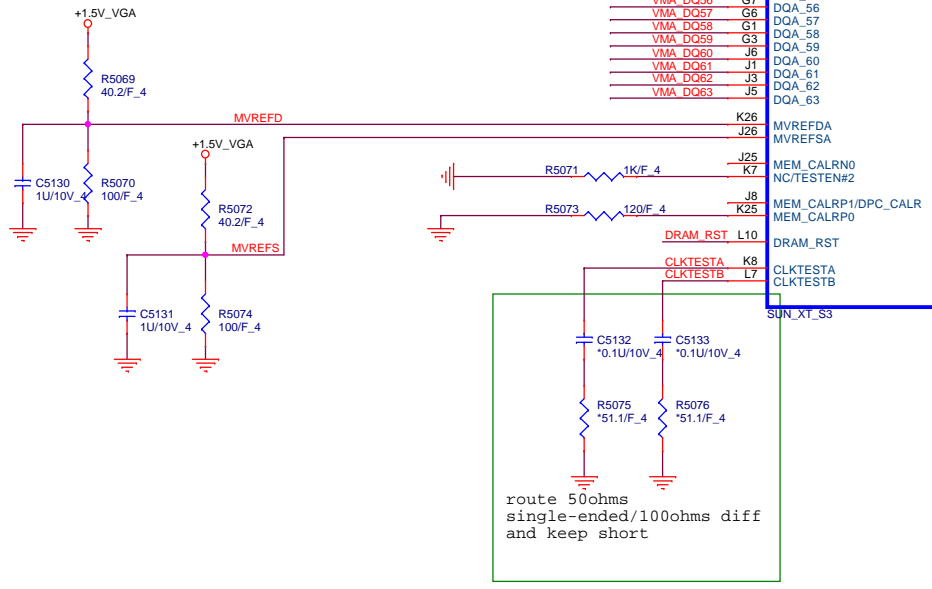


MEMORY INTERFACE



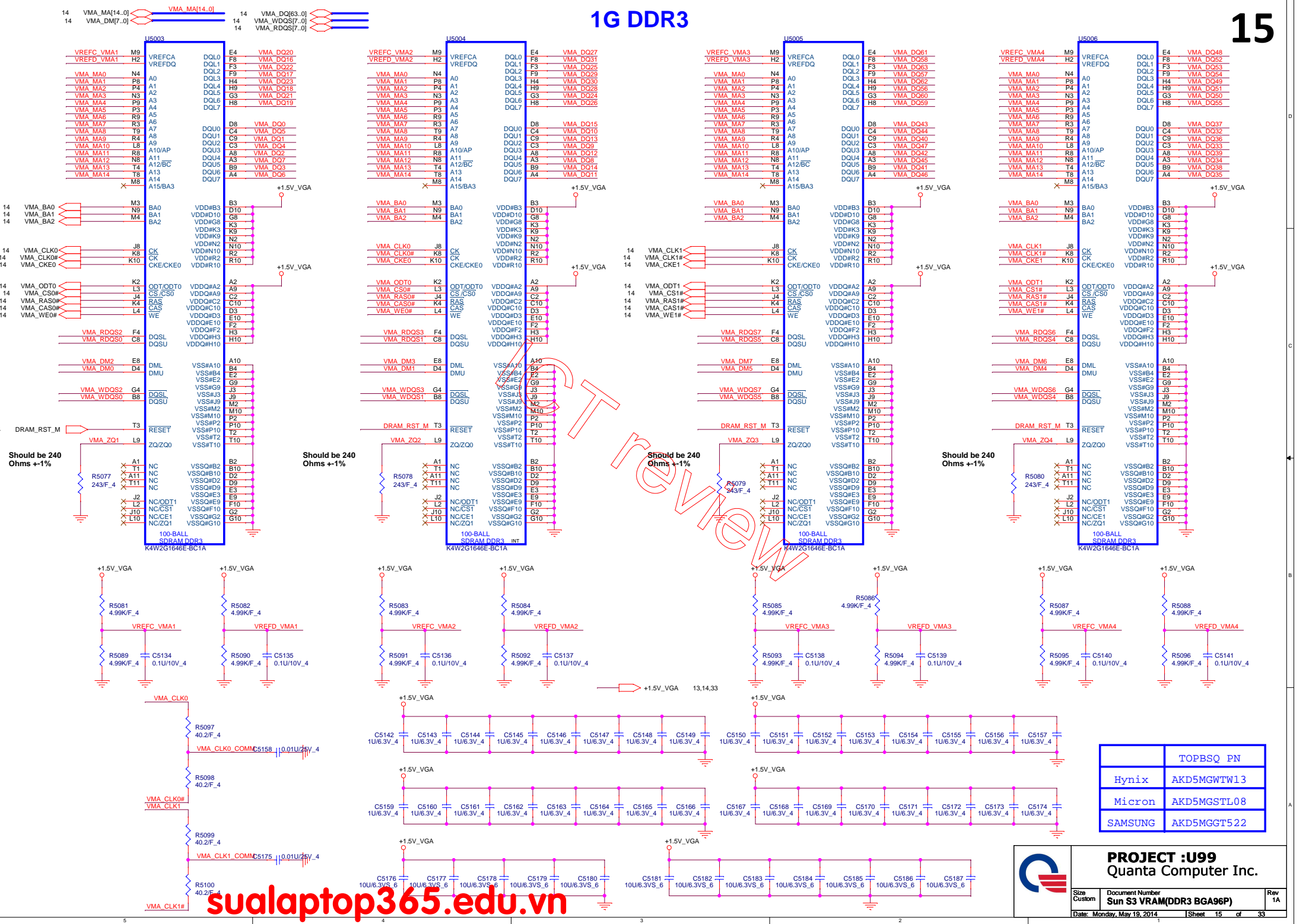
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.



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	Size Custom	Document Number Sun S3 MEM Interface
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1G DDR3



Review

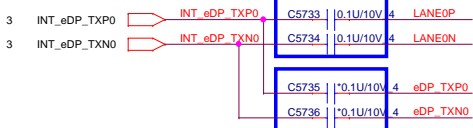
	TOPBSQ PN
Hynix	AKD5MGWTW13
Micron	AKD5MGSTL08
SAMSUNG	AKD5MGGT522

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Size	Document Number	Rev
Custom	Sun S3 VRAM(DDR3 BGA96P)	1A
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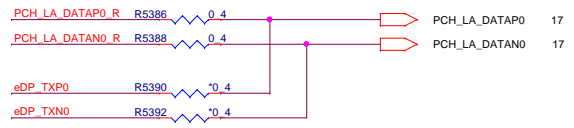
sualaptop365.edu.vn

for Bemma LVDS need stuff 0.1u cap ; need change 0.1u on next stage



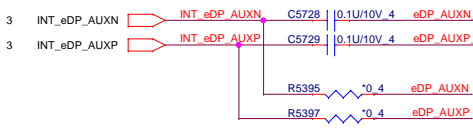
Bemba to LVDS Converter

From LVDS Converter



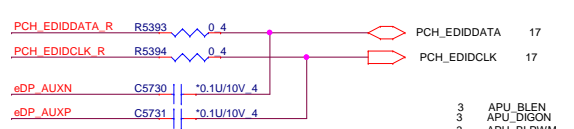
to Bemba eDP

from Bemba eDP



Bemba to LVDS Converter

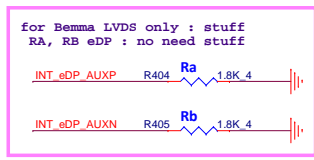
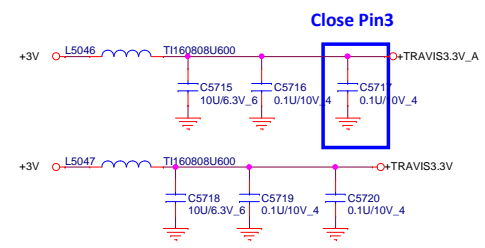
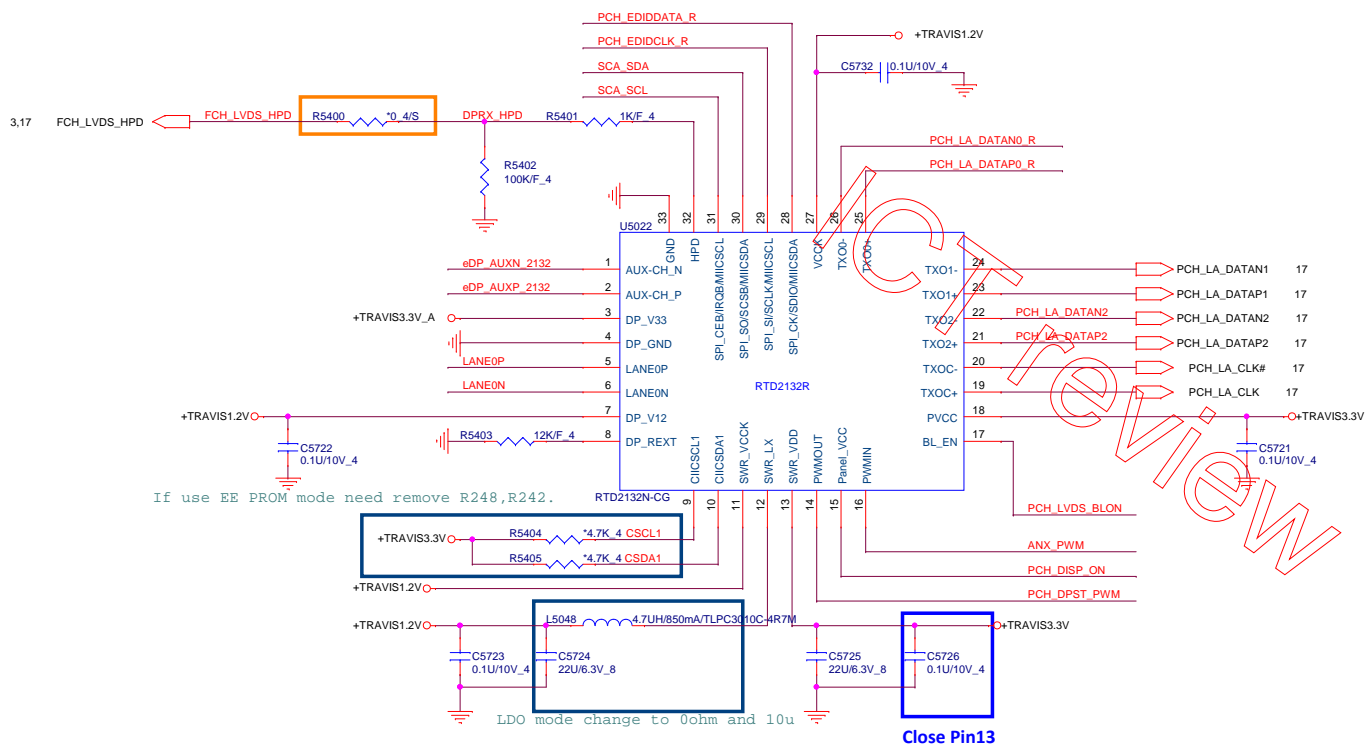
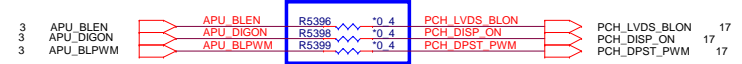
From LVDS Converter



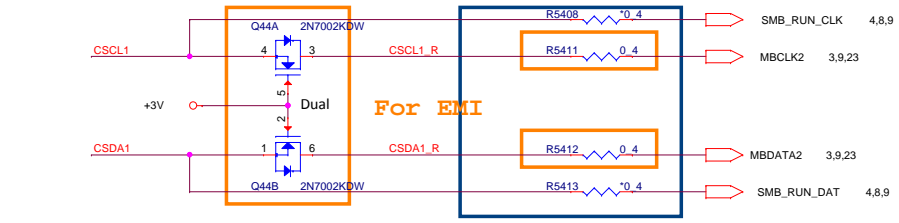
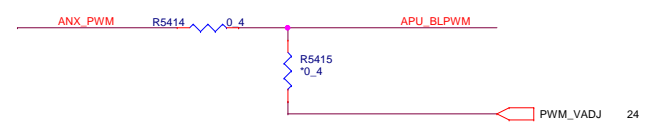
to Bemba eDP

from Bemba eDP

for Bemba eDP : stuff R5396 / R5398 / R5399
for Bemba LVDS : Don't stuff R5396 / R5398 / R5399



for Bemma LVDS only : stuff
RA, RB eDP : no need stuff
INT_eDP_AUXP R404 Ra
INT_eDP_AUXN R405 Rb



For EMI

EE PROM R5408, R5413
EC OPTION R5411, R5412

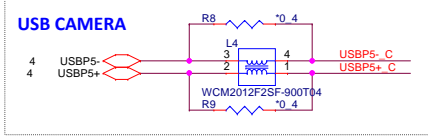
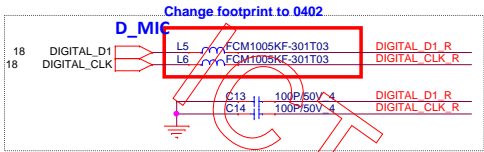
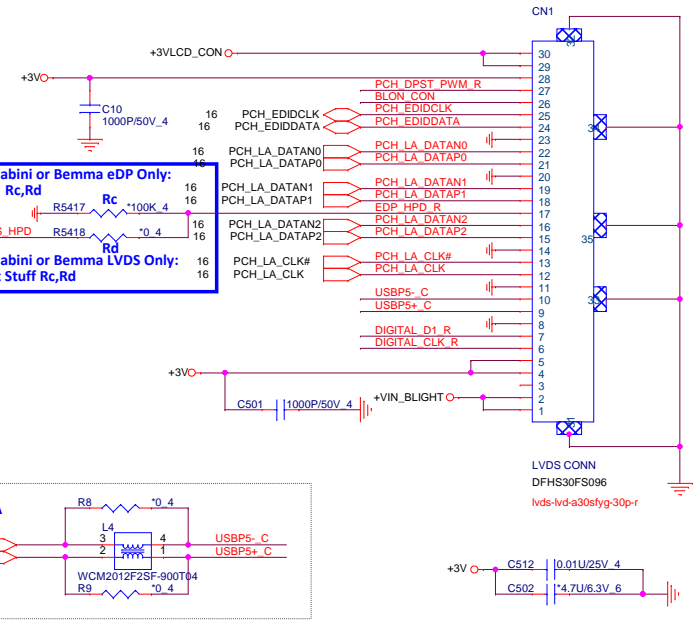
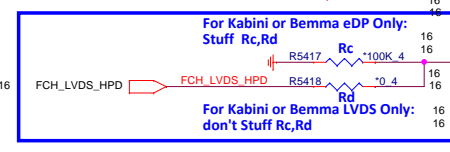
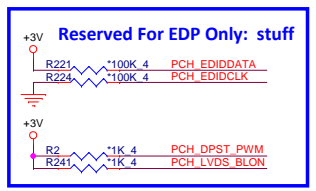
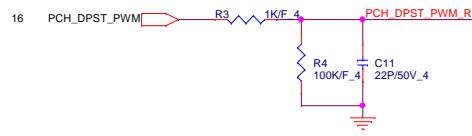
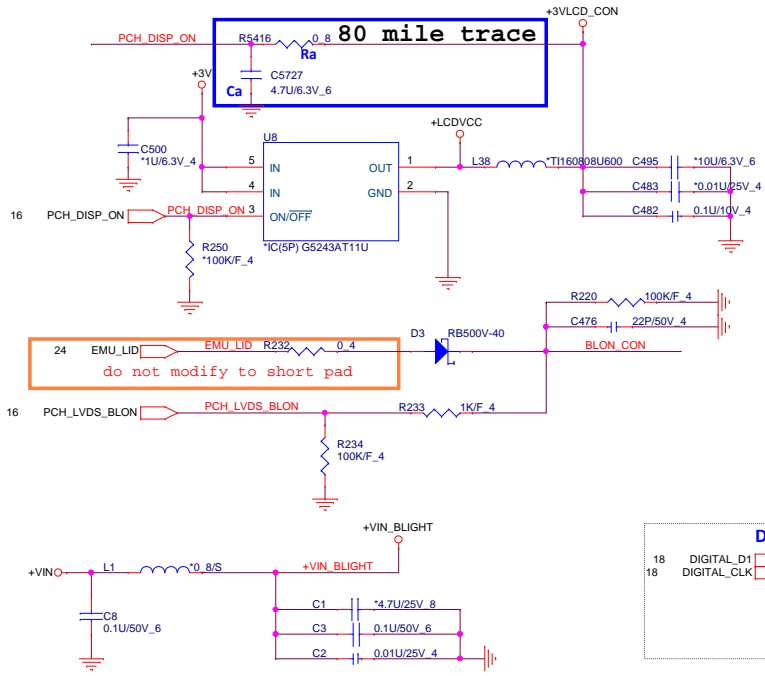
		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

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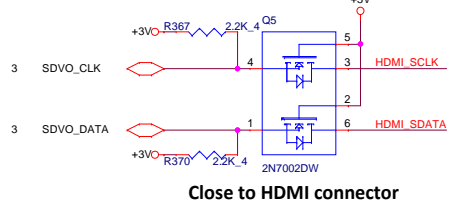
LVDS Conn.

for Bemma eDP : don't stuff Ra / Ca ;
for Bemma LVDS : stuff Ra / Ca



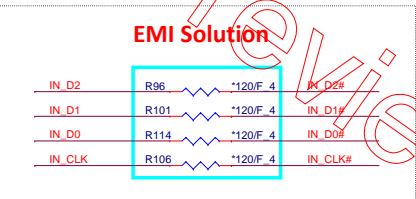
HDMI Conn.

HDMI SMBus Isolation

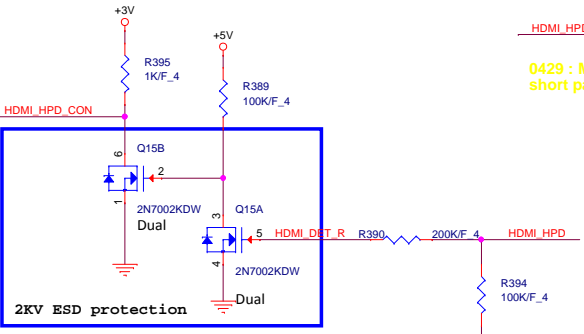


Close to HDMI connector

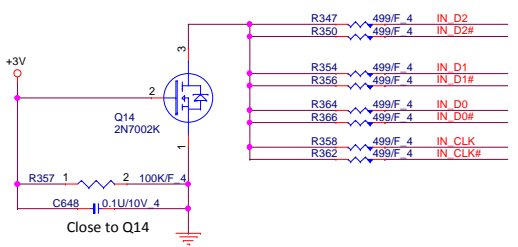
EMI Solution



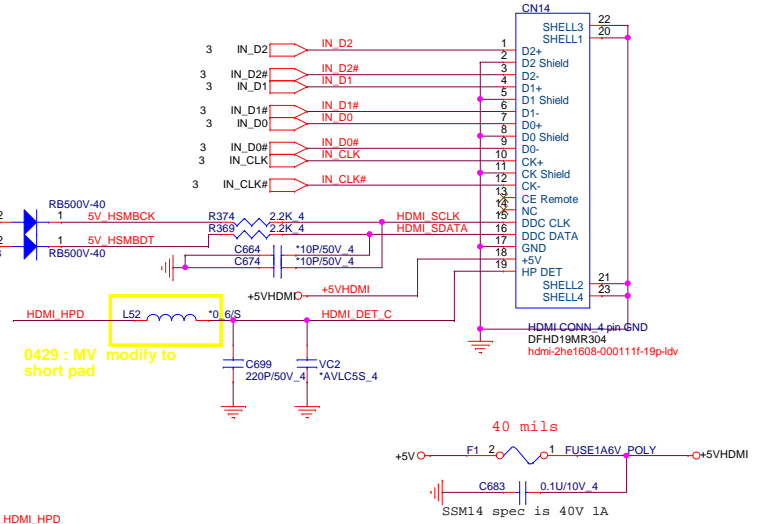
HDMI HPD SENSE



0429 : MV modify to short pad

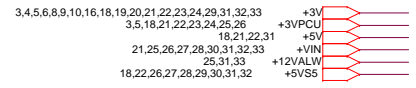


Close to Q14



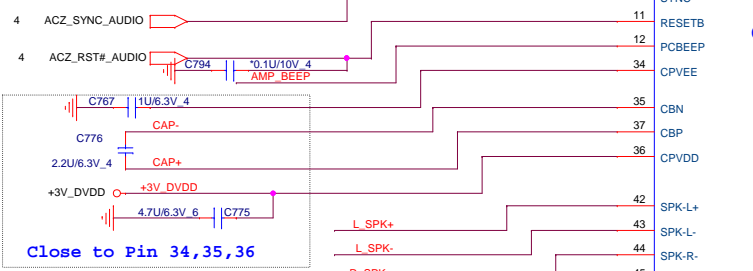
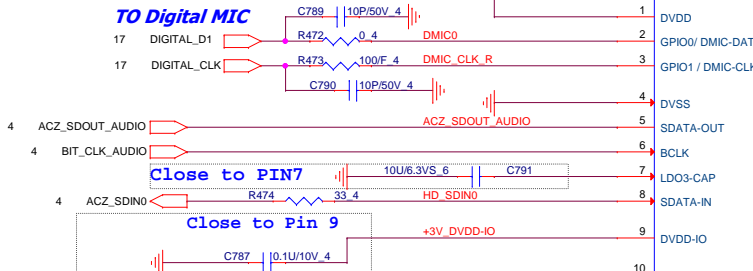
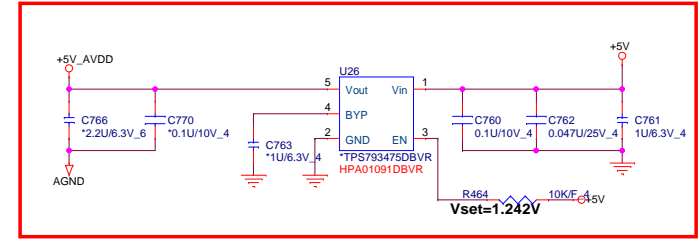
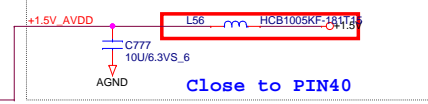
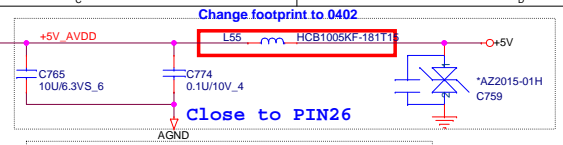
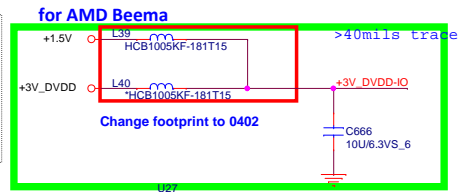
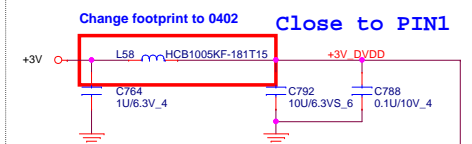
40 mils

SSM14 spec is 40V 1A

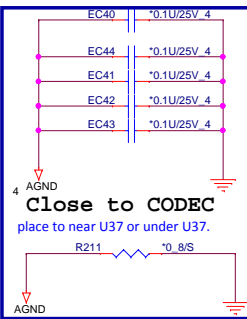
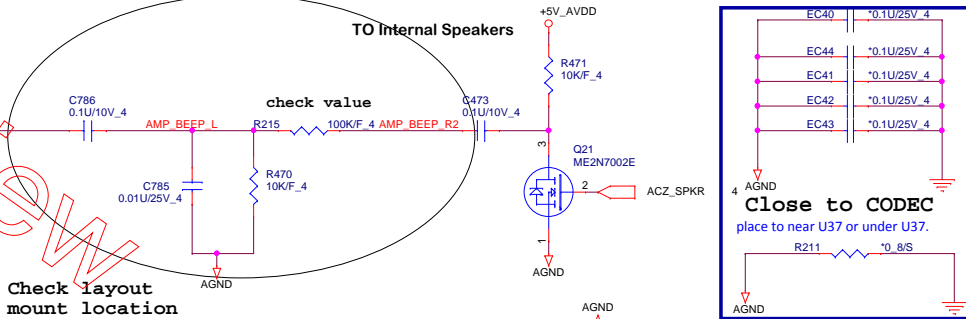
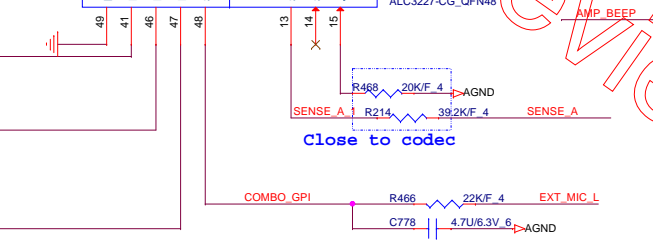
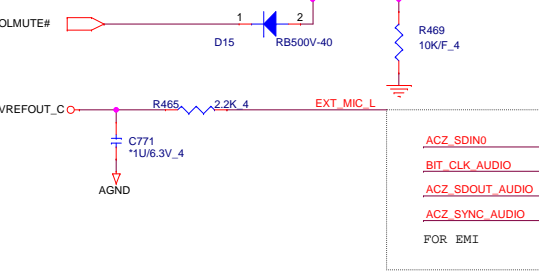
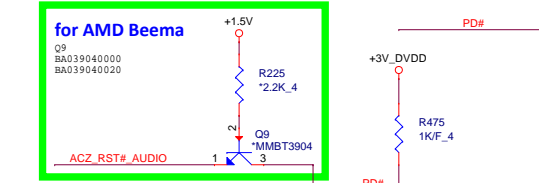
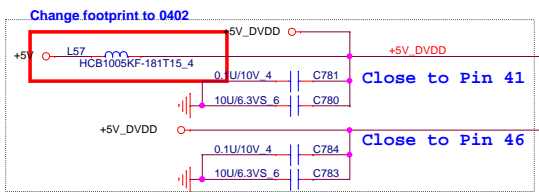
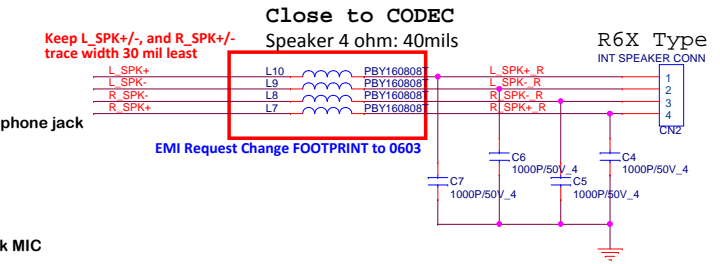
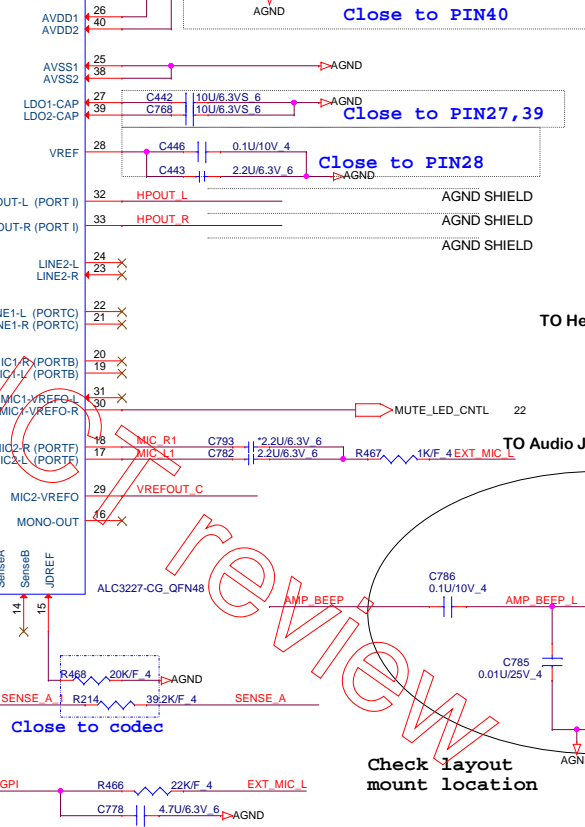


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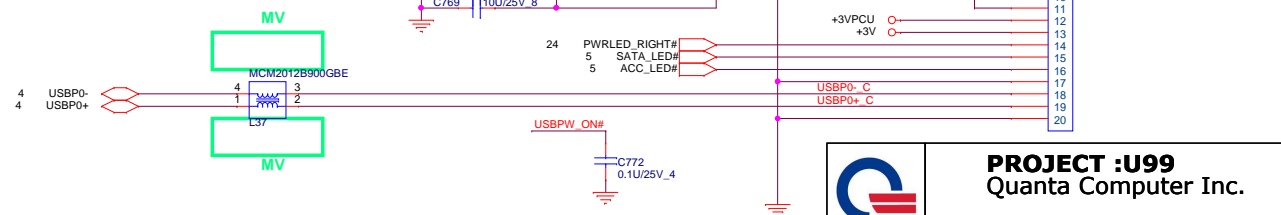
Size Custom	Document Number LCD Connector (LVDS)	Rev 3A
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Analog
Digital



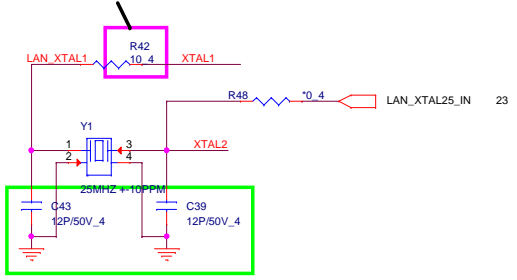
USB 2.0 AND AUDIO COMBO JACK



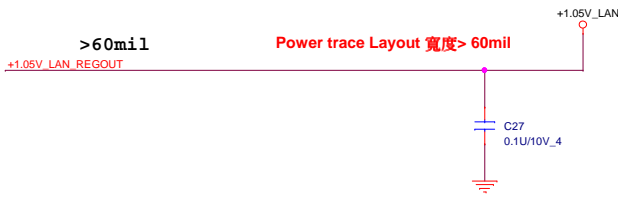
PROJECT :U99
Quanta Computer Inc.

Size Custom	Document Number Azalia ALC3227	Rev 1A
Date: Monday, May 19, 2014	Sheet 18 of 33	

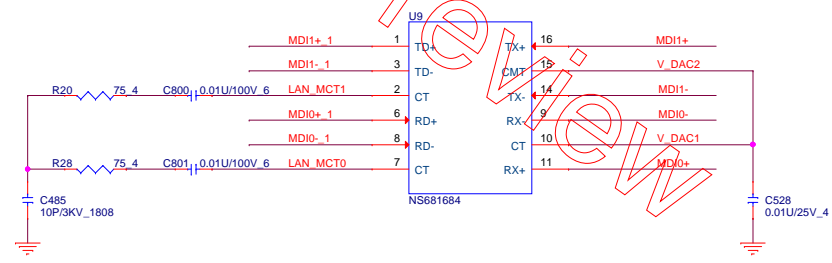
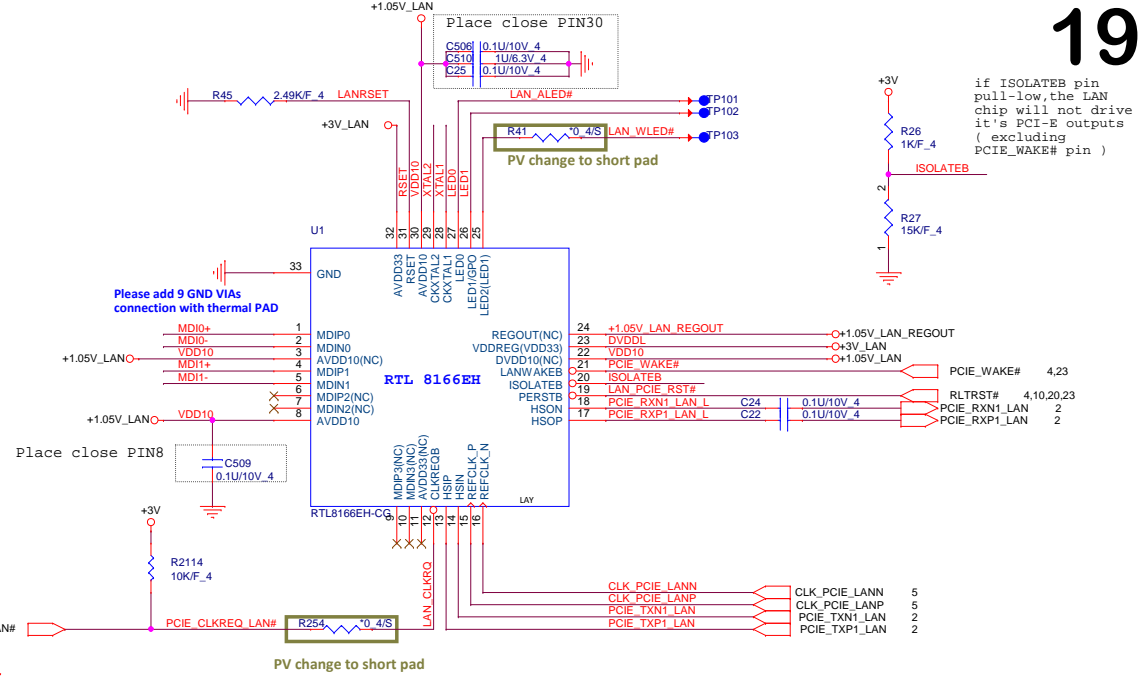
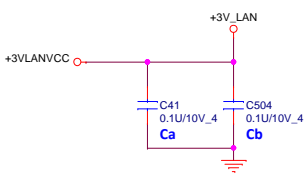
For EMI 0 ~ 22 ohm



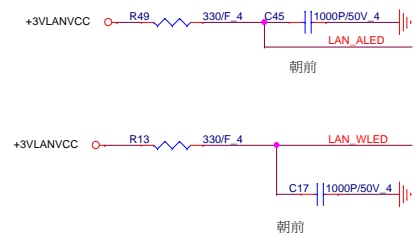
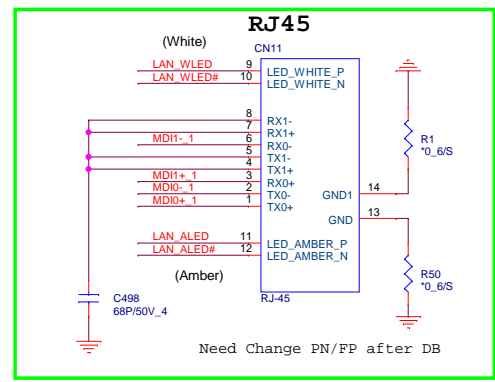
SI change to 12p



Place close PIN23 and PIN32

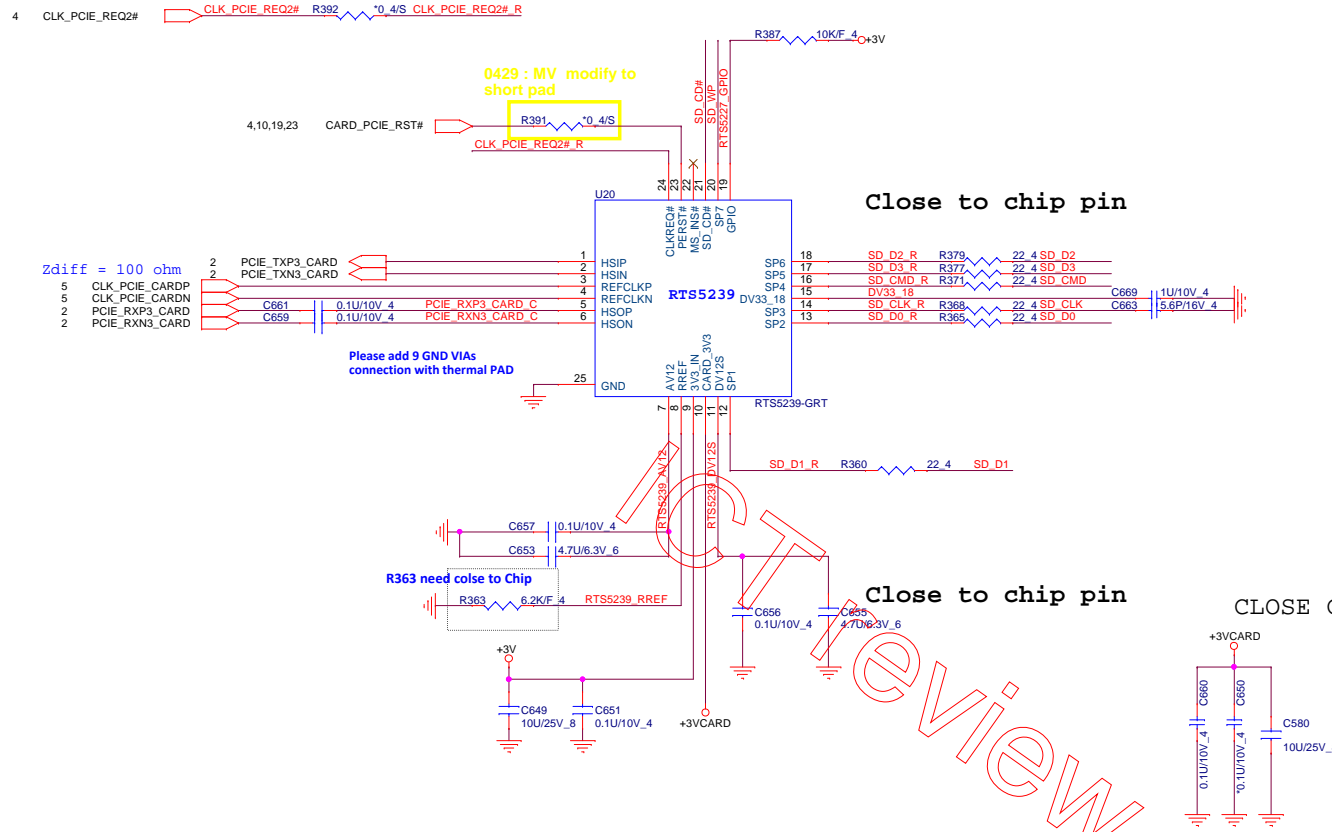


LAN conn



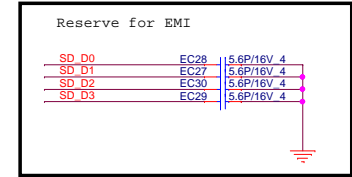
3,4,5,6,8,9,10,16,17,18,20,21,22,23,24,29,31,32,33
+3V
+3VLANVCC

			PROJECT :U99 Quanta Computer Inc.	
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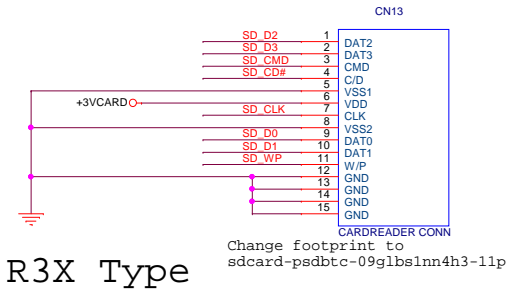


SP1	SD_D1	MS_D1
SP2	SD_D0	MS_D0
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS

Share Pin



SD / MMC
CARD READER

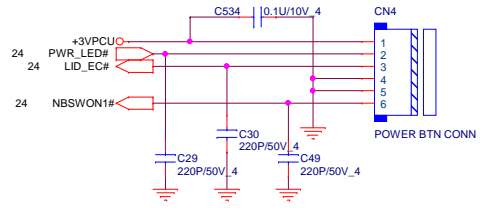


R3X Type

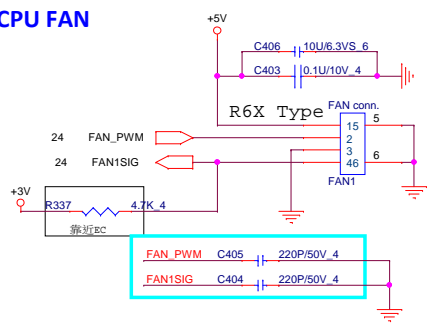
	PROJECT :U99 Quanta Computer Inc.		Rev
	Size	Document Number	1A
	Custom	RT5239 & CR SOCKET	
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Power Button Connector

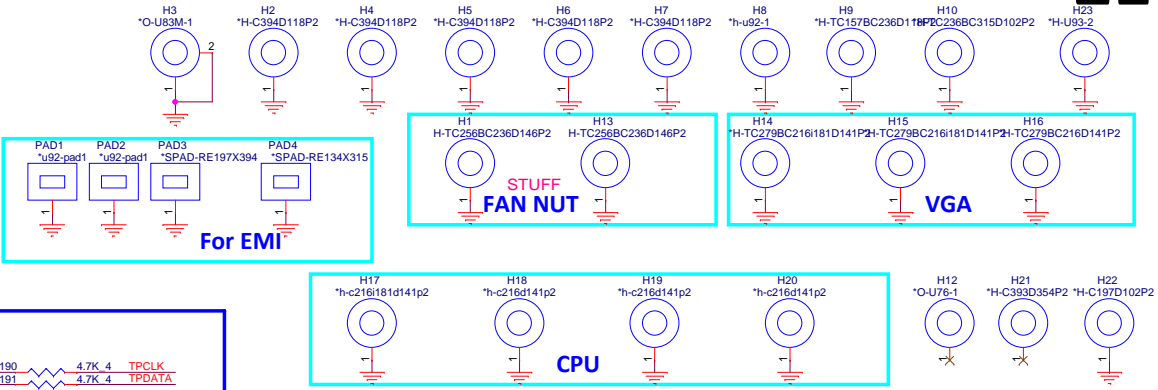
Pin1 : +3VPCU(LIDSWITCH PWR)
 Pin2 : POWER LED
 Pin3 : LIDSWITCH
 Pin4 : GND
 Pin5 : GND
 Pin6 : POWERON#



CPU FAN

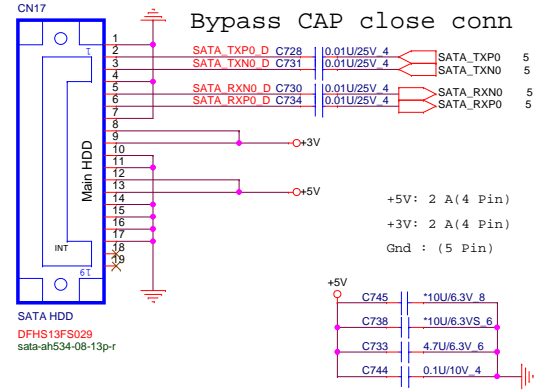


Hole

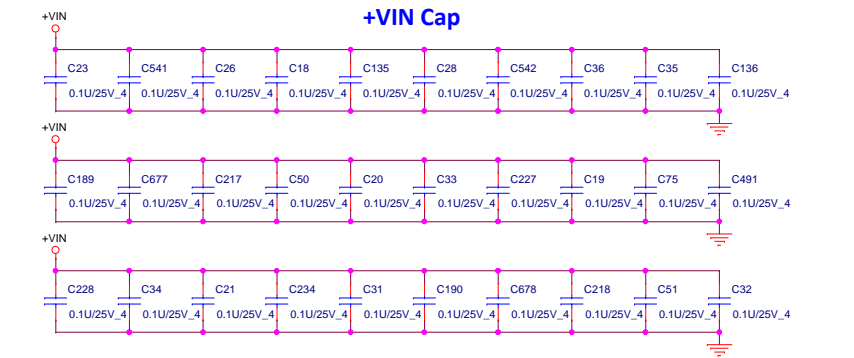
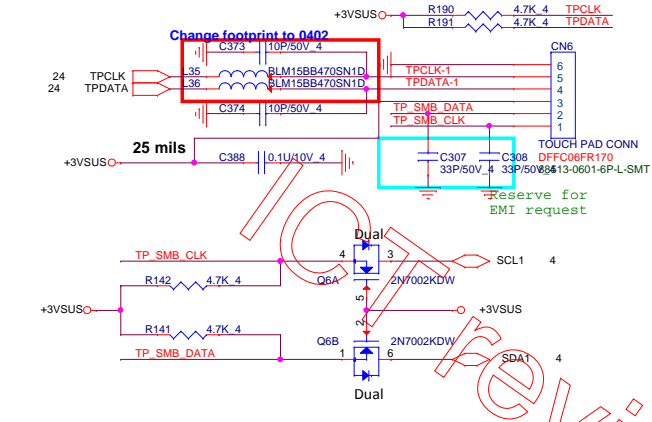


SATA HDD Connector(Cable type)

Bypass CAP close conn

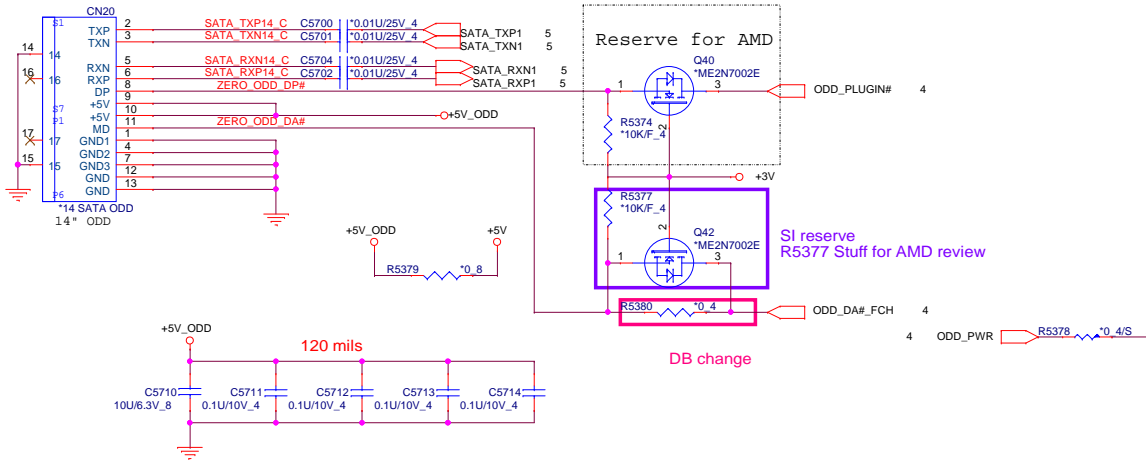


Touch Pad



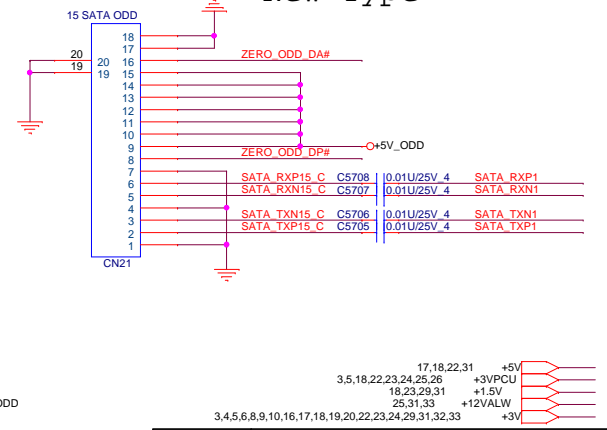
SATA ODD CONNECTOR

14" SATA ODD Bypass CAP close conn



15" SATA ODD

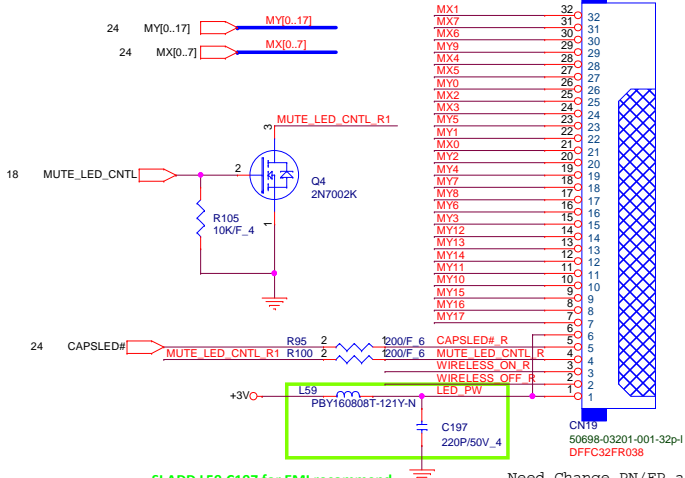
New Type



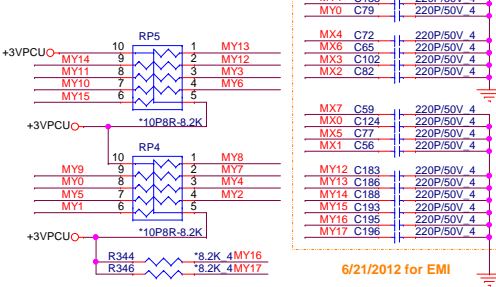
PROJECT :U99
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Size Custom	Document Number	Rev 1A
SATA HDD/ODD/MSATA CONN		
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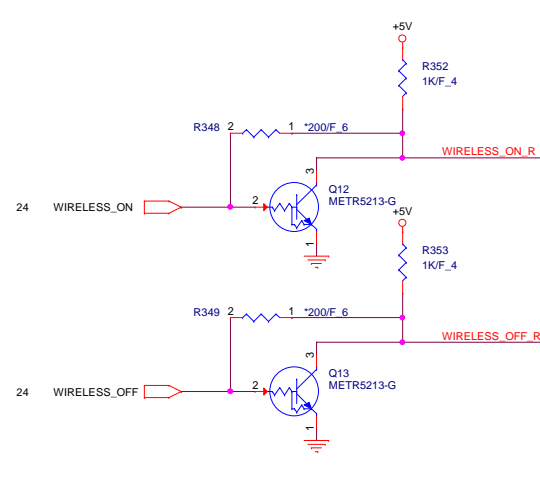
KEYBOARD Con.



KEYBOARD PULL-UP



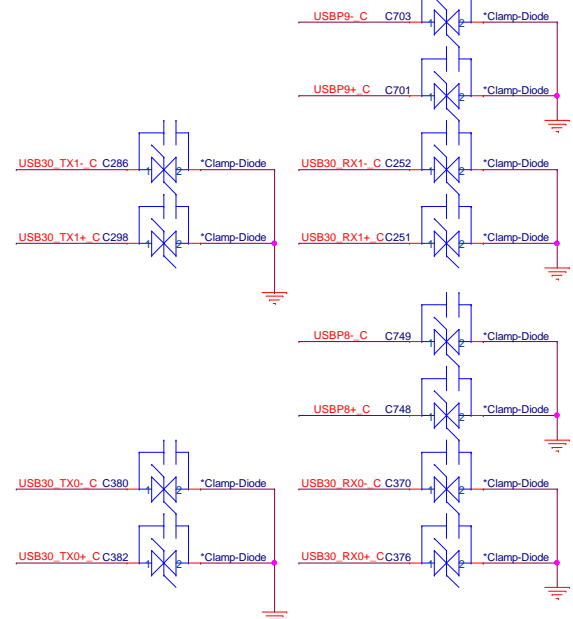
MY5	C106	220P/50V_4
MY6	C157	220P/50V_4
MY3	C179	220P/50V_4
MY7	C143	220P/50V_4
MY8	C153	220P/50V_4
MY9	C69	220P/50V_4
MY10	C192	220P/50V_4
MY11	C191	220P/50V_4
MY1	C119	220P/50V_4
MY2	C130	220P/50V_4
MY4	C133	220P/50V_4
MY0	C79	220P/50V_4
MX4	C72	220P/50V_4
MX6	C65	220P/50V_4
MX3	C102	220P/50V_4
MX2	C82	220P/50V_4
MX7	C59	220P/50V_4
MX0	C124	220P/50V_4
MX5	C77	220P/50V_4
MX1	C56	220P/50V_4
MY12	C183	220P/50V_4
MY13	C186	220P/50V_4
MY14	C188	220P/50V_4
MY15	C193	220P/50V_4
MY16	C195	220P/50V_4
MY17	C196	220P/50V_4



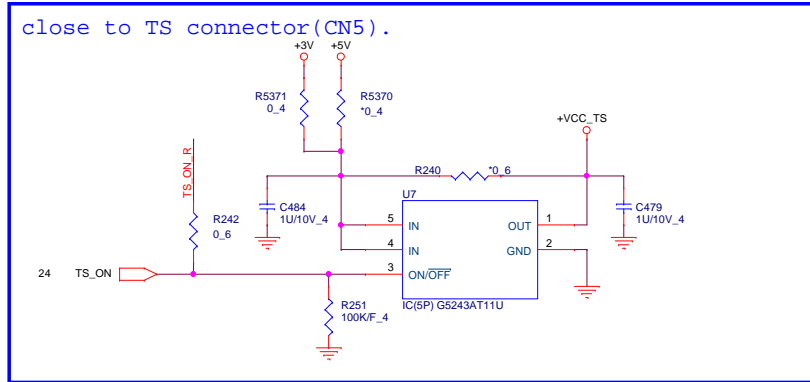
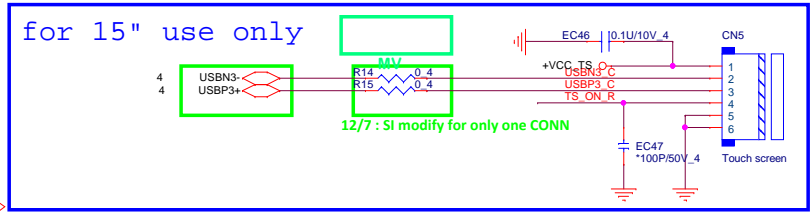
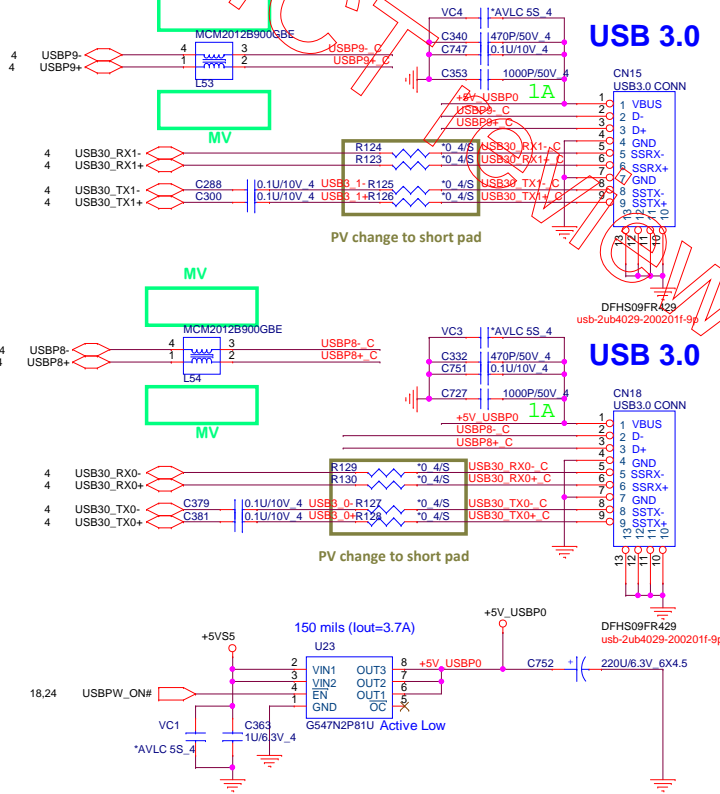
SI ADD L59,C197 for EMI recommend Need Change PN/FP after DB

NM9 Type

USB 2.0/3.0 Combo



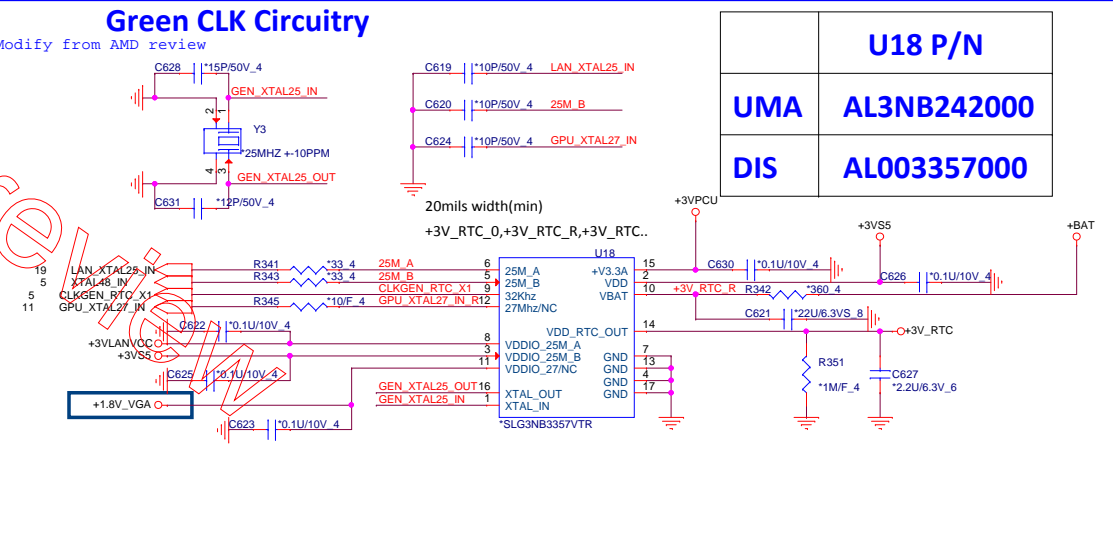
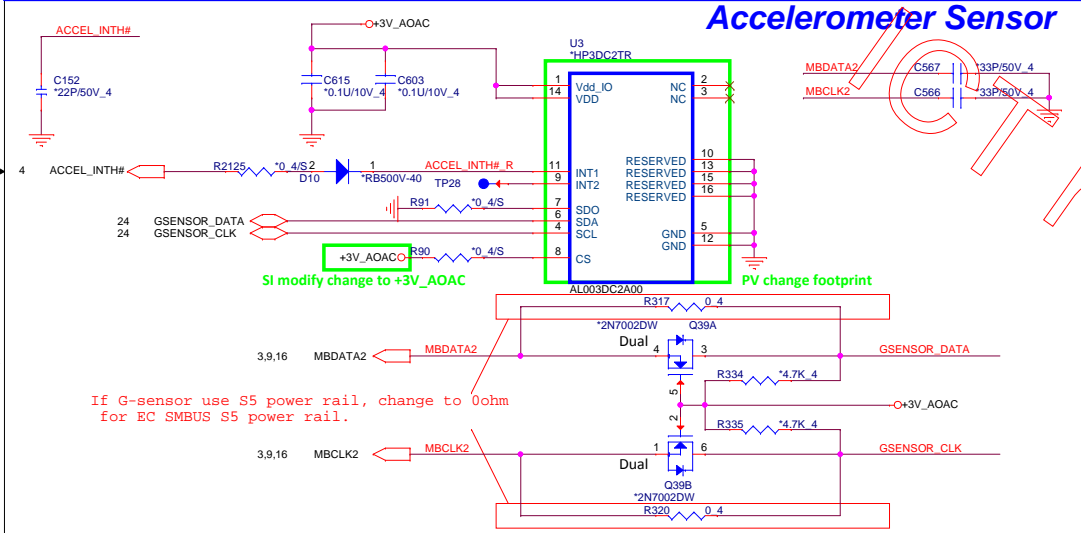
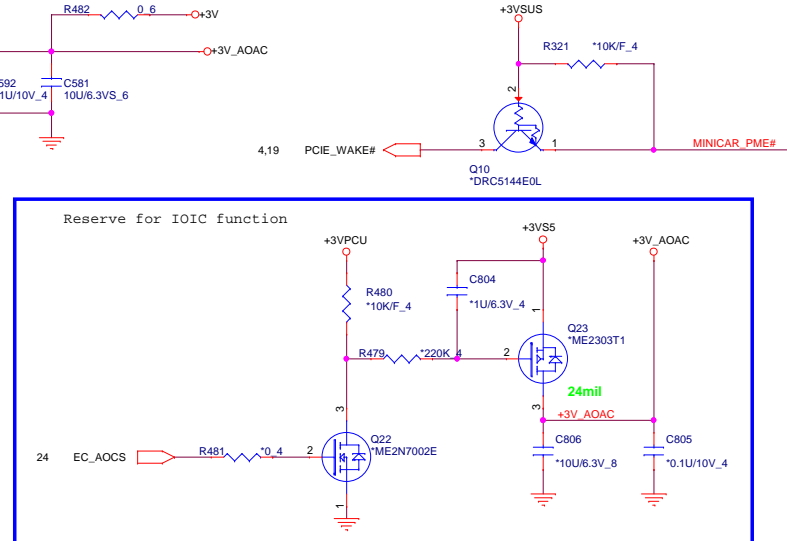
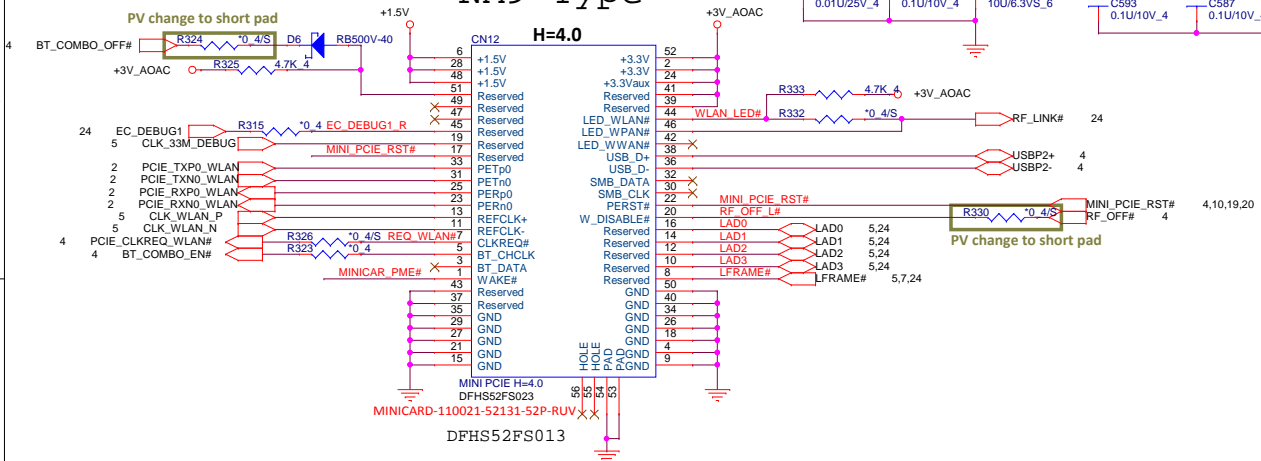
SPS Type



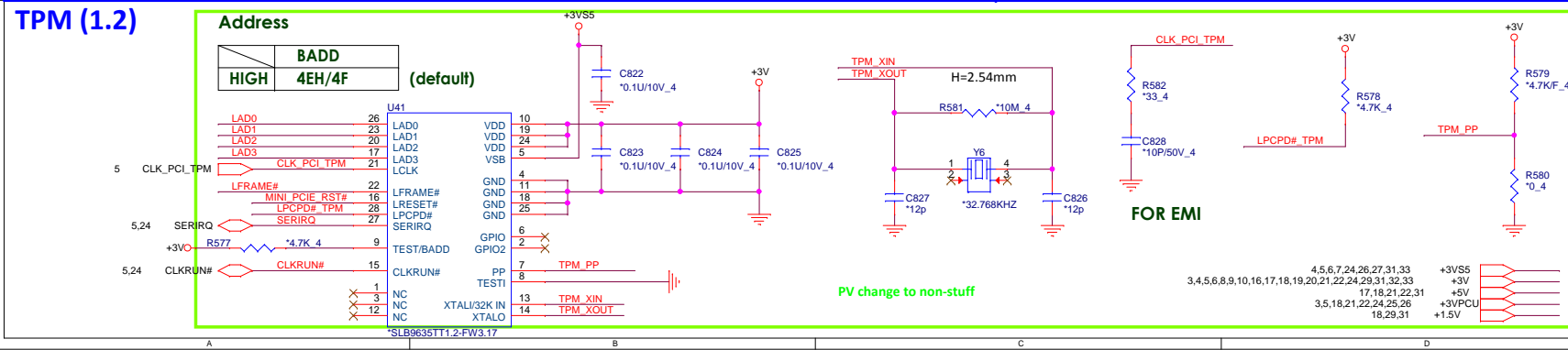
PROJECT :U99
Quanta Computer Inc.

Size Custom	Document Number USB 3.0/KB/Green CLK	Rev 1A
Date: Monday, May 19, 2014	Sheet 22of	33

Mini Card
WLAN/BT(Optional)



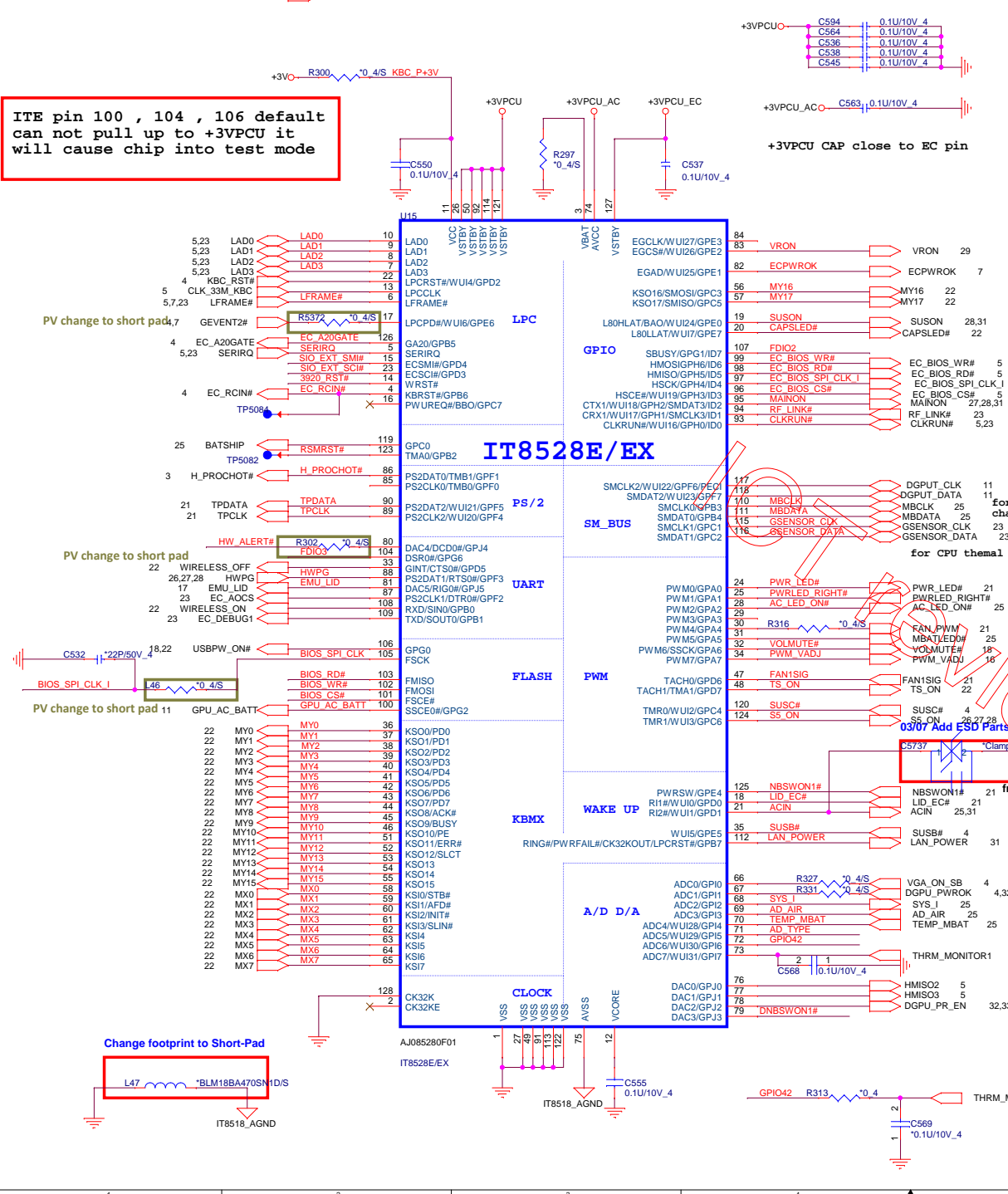
U18 P/N	
UMA	AL3NB242000
DIS	AL003357000



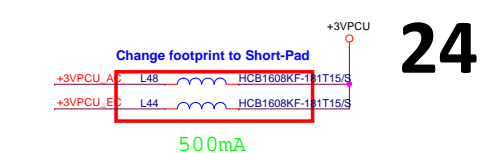
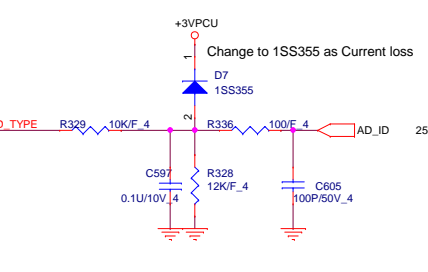
PROJECT :U99 Quanta Computer Inc.		
Size Document Number MINI-PCIE/LED	Date: Monday, May 19, 2014	Rev 1A

3,4,5,6,8,9,10,16,17,18,19,20,21,22,23,29,31,32,33
3,5,18,21,22,23,25,26

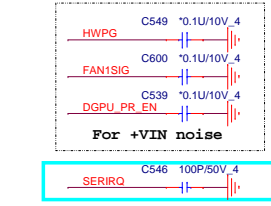
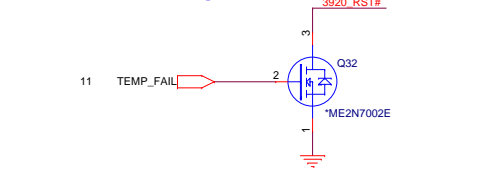
ITE pin 100 , 104 , 106 default can not pull up to +3VPCU it will cause chip into test mode



Smart adapter Type check

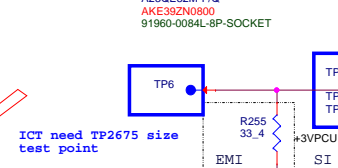
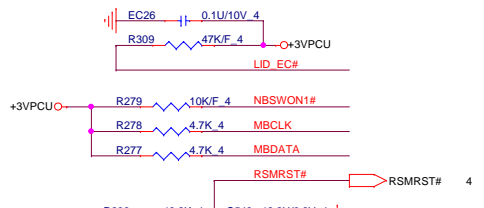
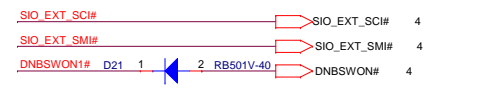
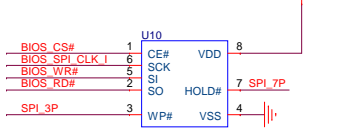


DGPU Thermal protect

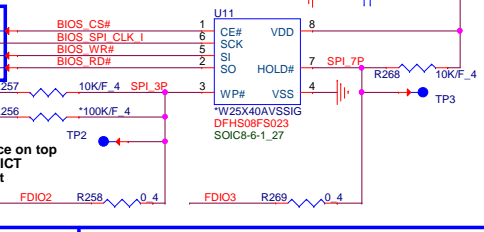


Vender	Size	P/N
AIT	4M	AKE39ZN0800
EON	4M	AKE39ZN0Q03
WND	4M	AKE39FN0N01
Socket		DFHS08FS023

4M SPI EC ROM



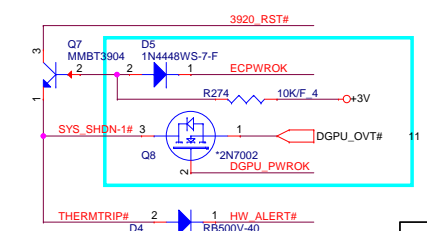
128K byte SPI EC ROM



Adapter select

H1 ==> A6-5200 25W CPU + DIS
Low ==>UMA/DIS/SG

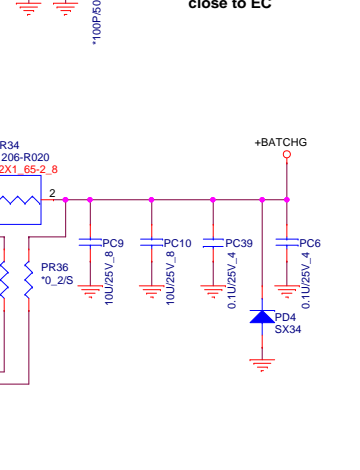
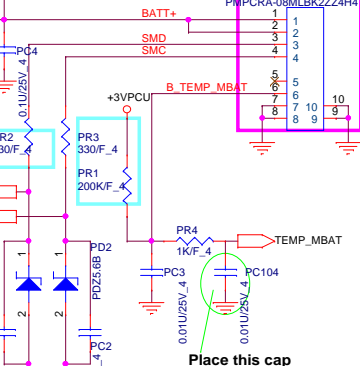
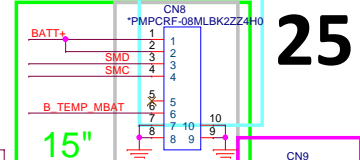
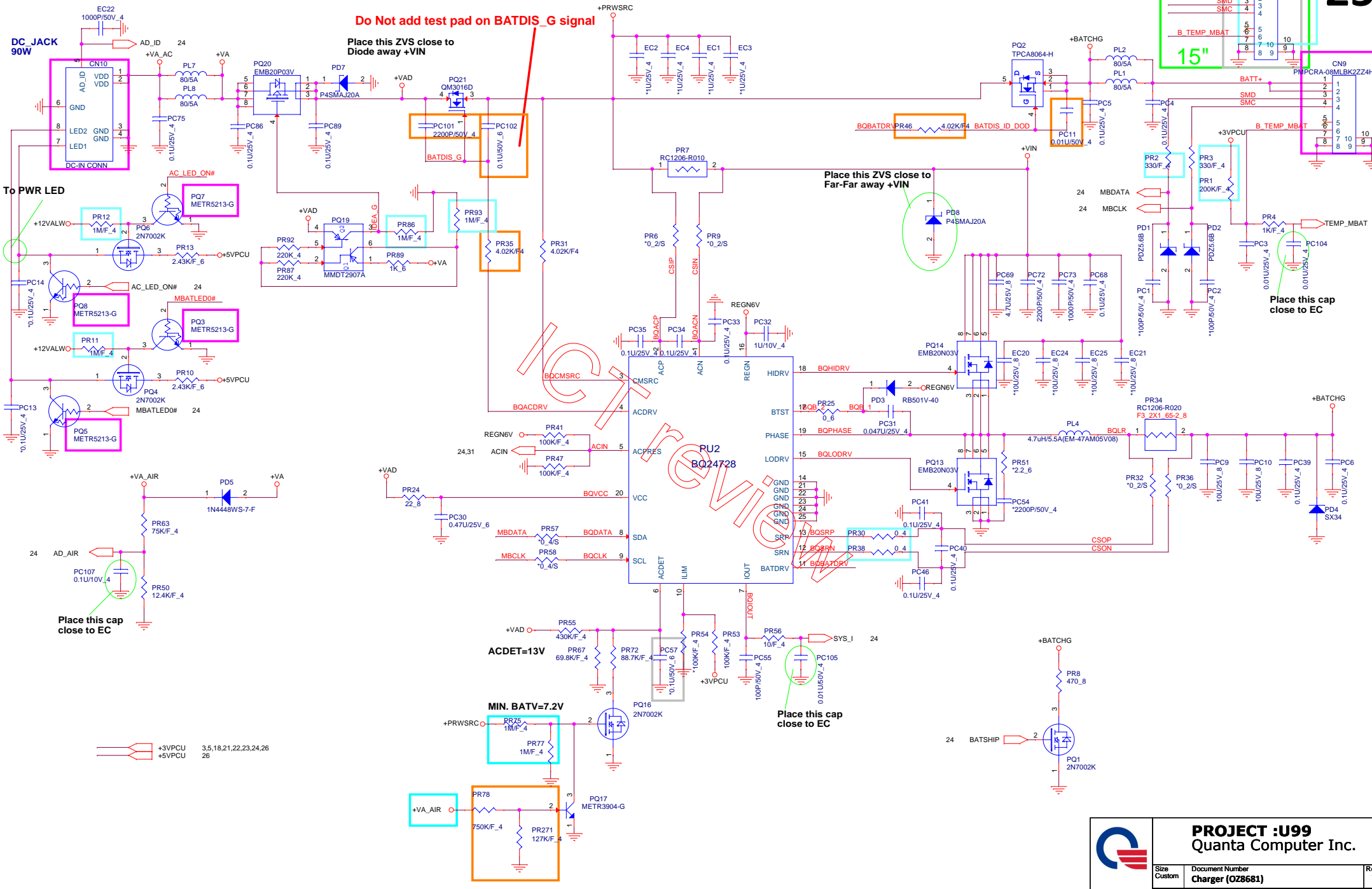
Platform model	GPIO42	adapter
A6 25W CPU + DIS	High	90W
DIS/SG/UMA	Low	65W



PROJECT :U99
Quanta Computer Inc.

Size Custom	Document Number EC (IT8528E)/ROM	Rev 1A
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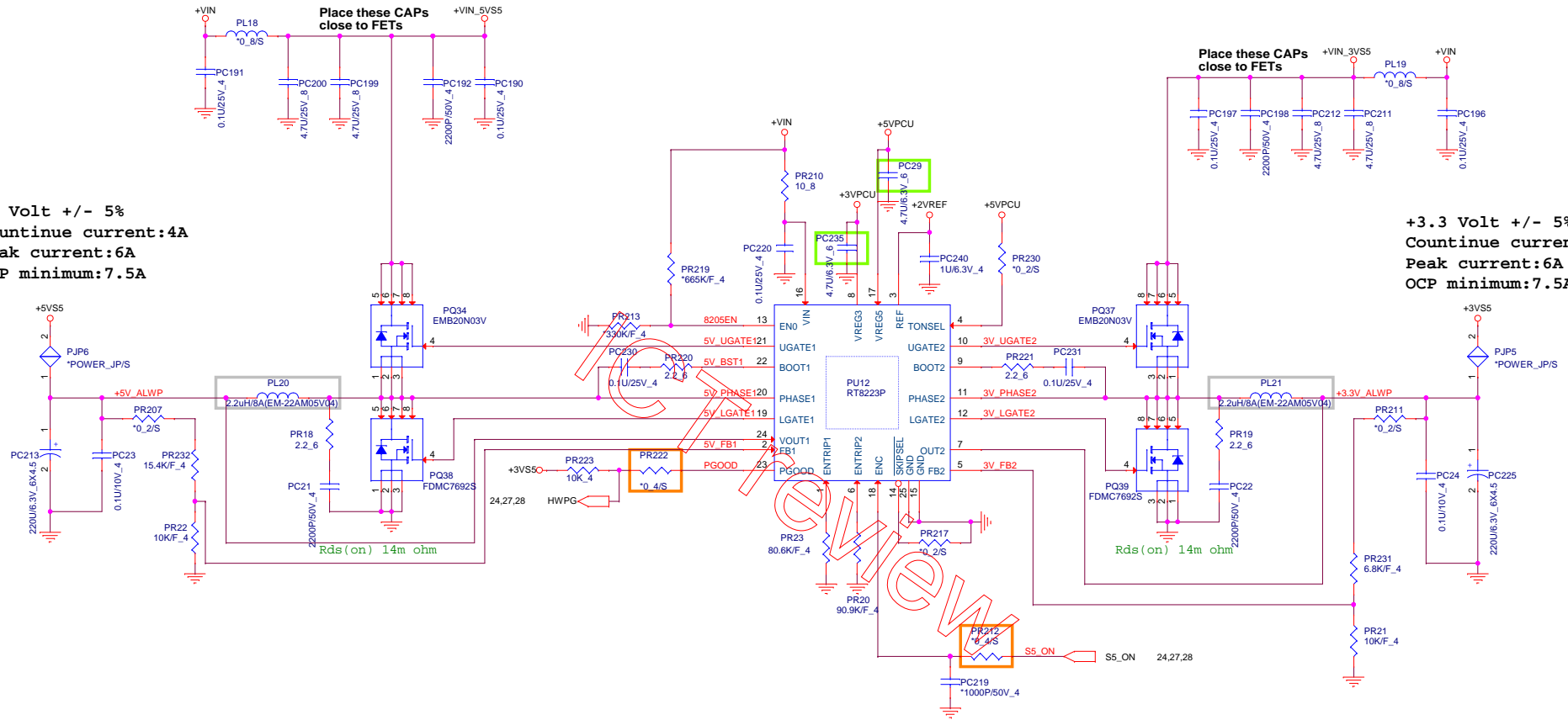
Date: Monday, May 19, 2014 | Sheet 24 of 33




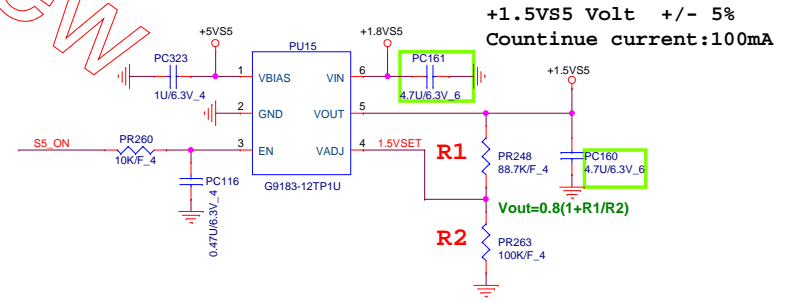
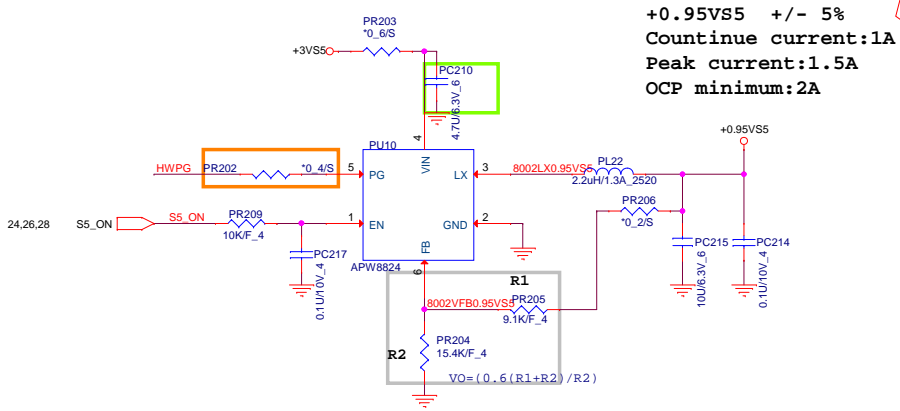
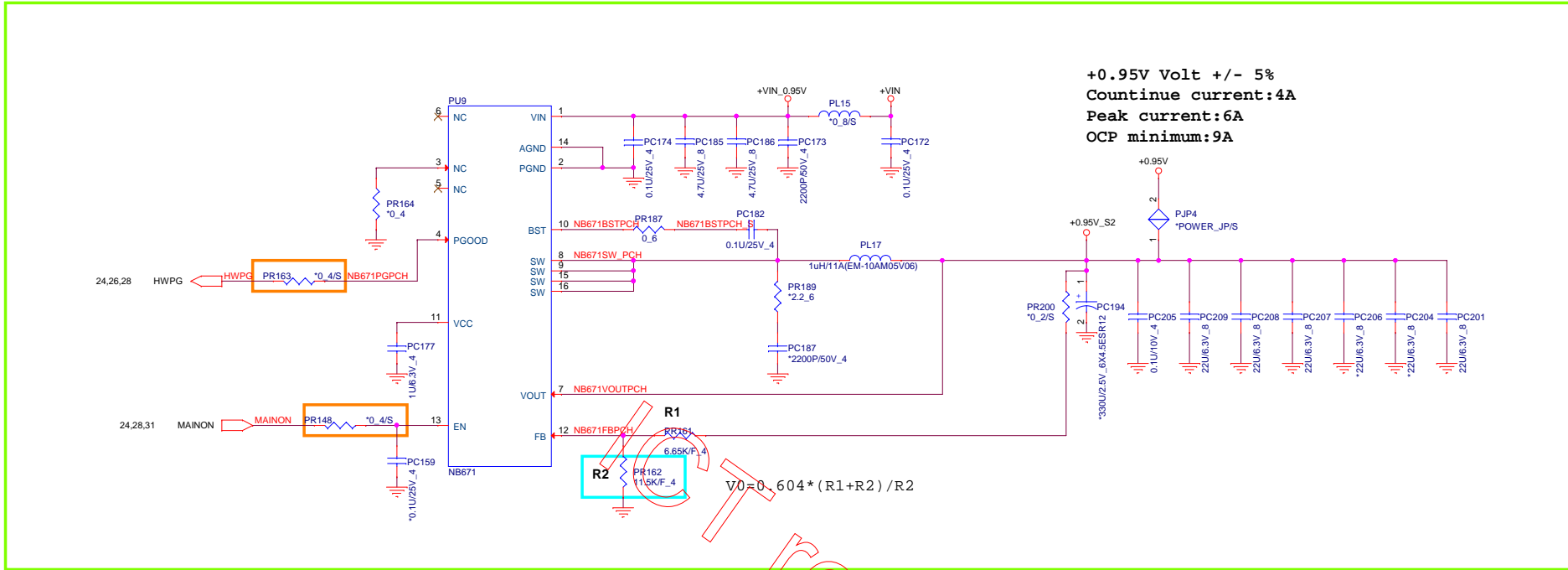
			PROJECT :U99		
			Quanta Computer Inc.		
Size Custom	Document Number Charger (028681)	Rev 1A			
Date: Monday, May 19, 2014	Sheet 25	of 33			


+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

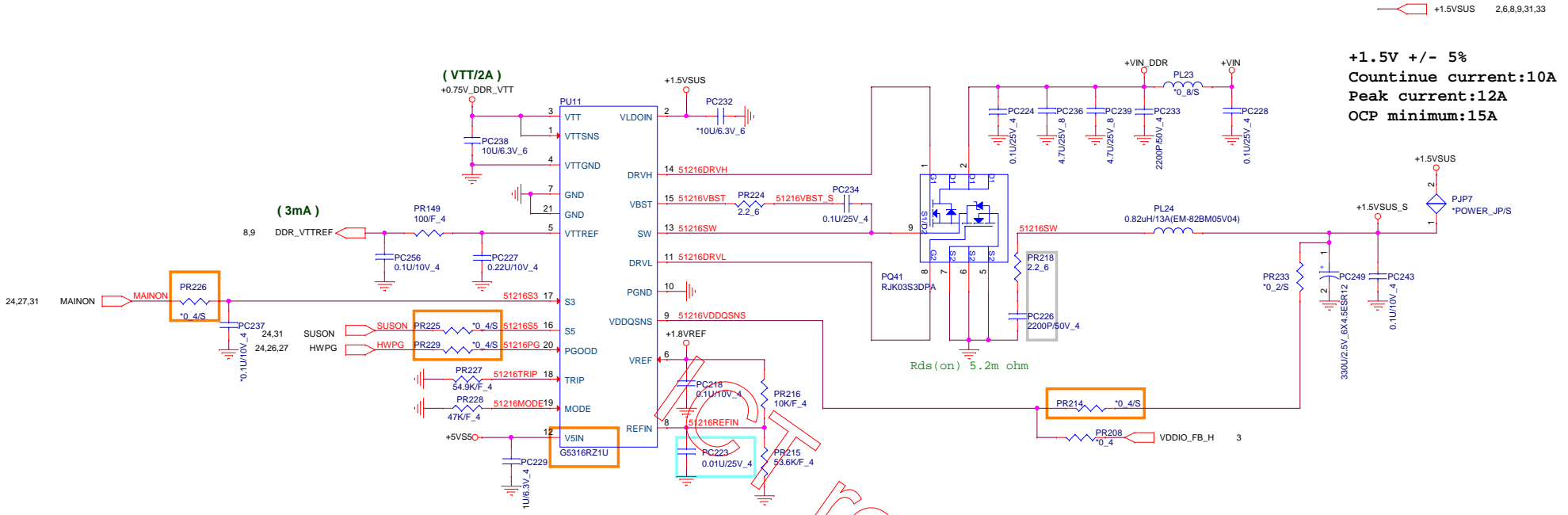
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



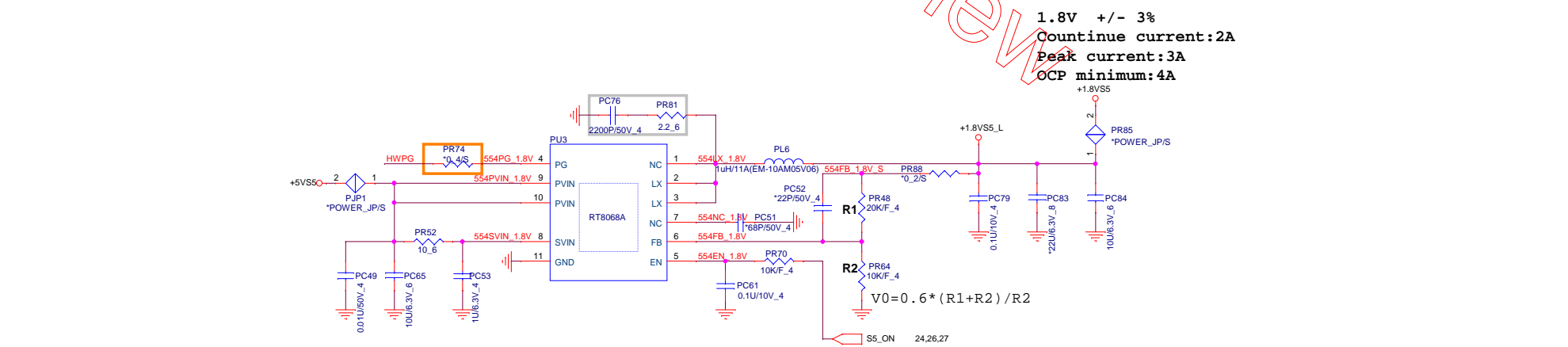
	PROJECT :U99		
	Quanta Computer Inc.		
	Size Custom	Document Number 3/5VPCU(RT8223P)	Rev 1A
Date: Monday, May 19, 2014	Sheet	26	of 33



 PROJECT :U99 Quanta Computer Inc.			
			Size Custom
Date: Monday, May 19, 2014			Sheet 27 of 33



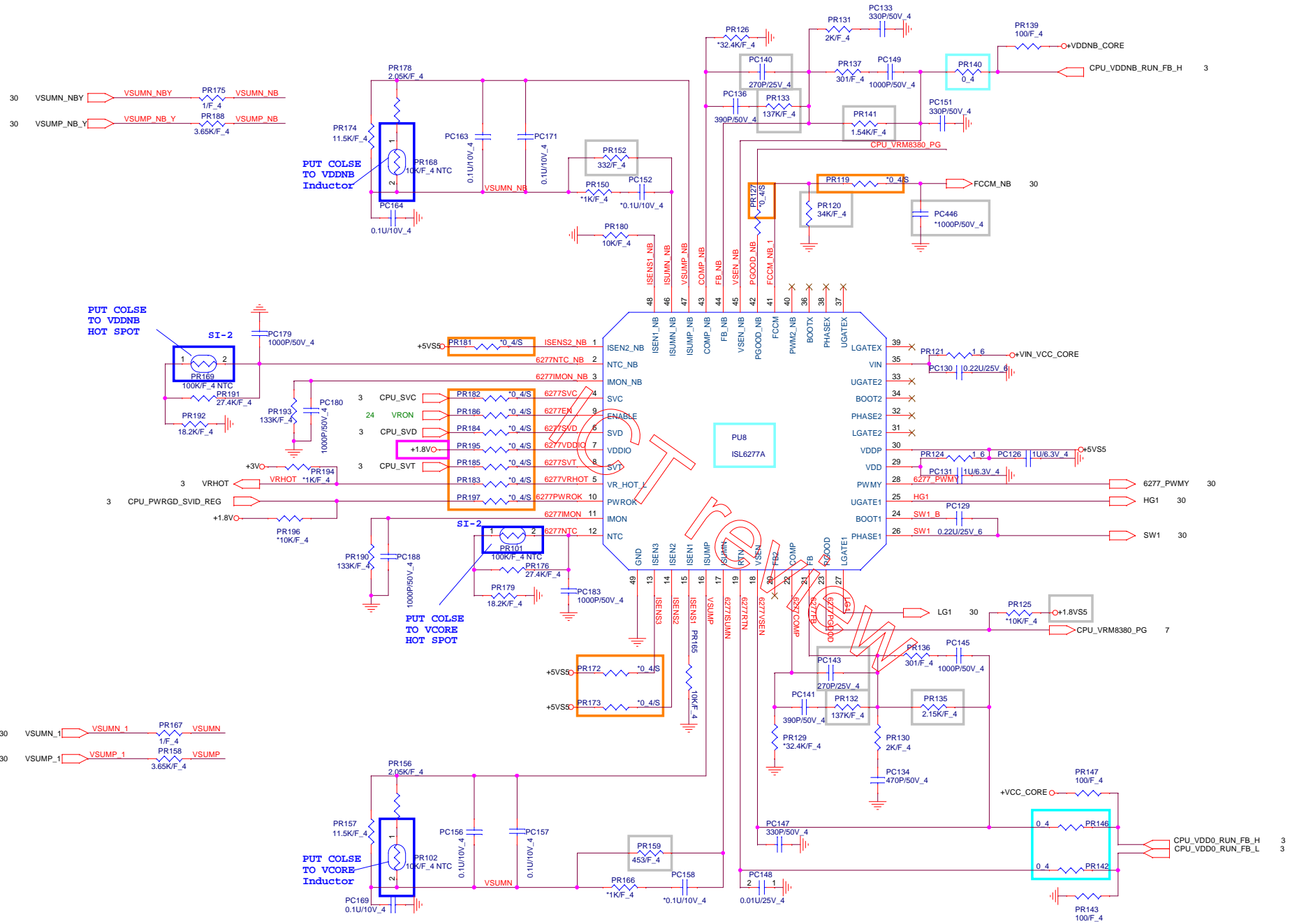
+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCP minimum:15A




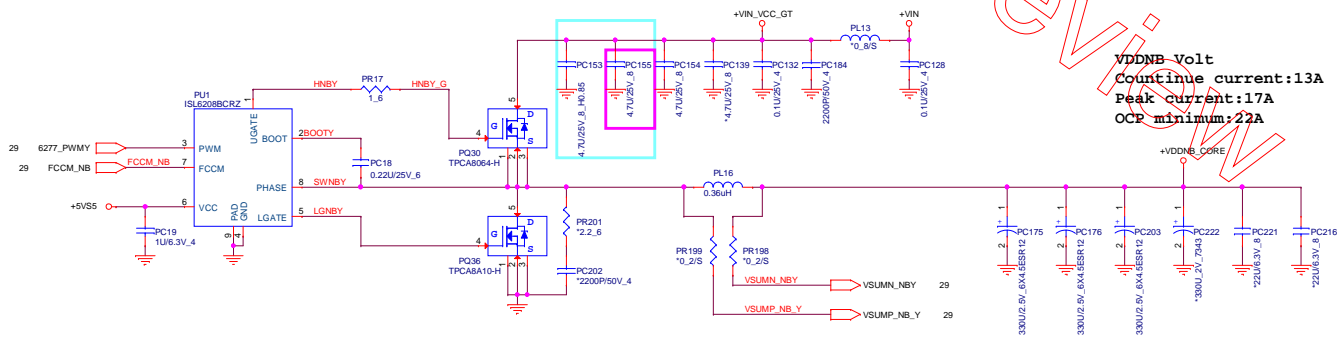
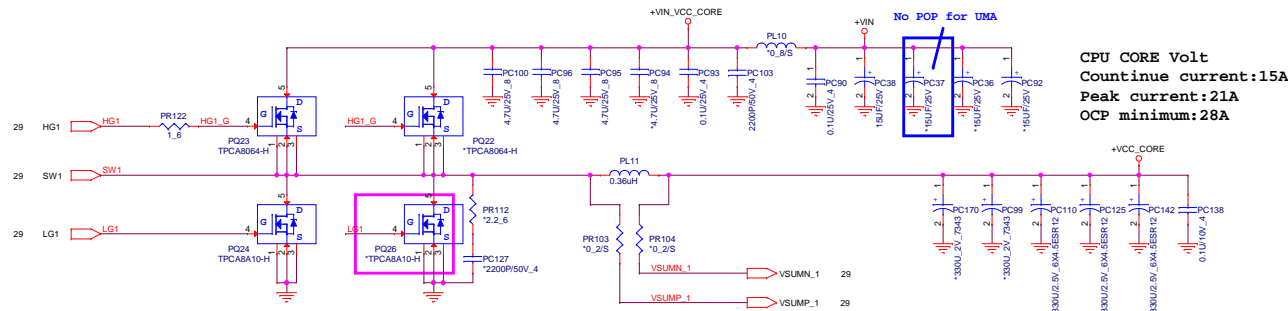
1.8V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A

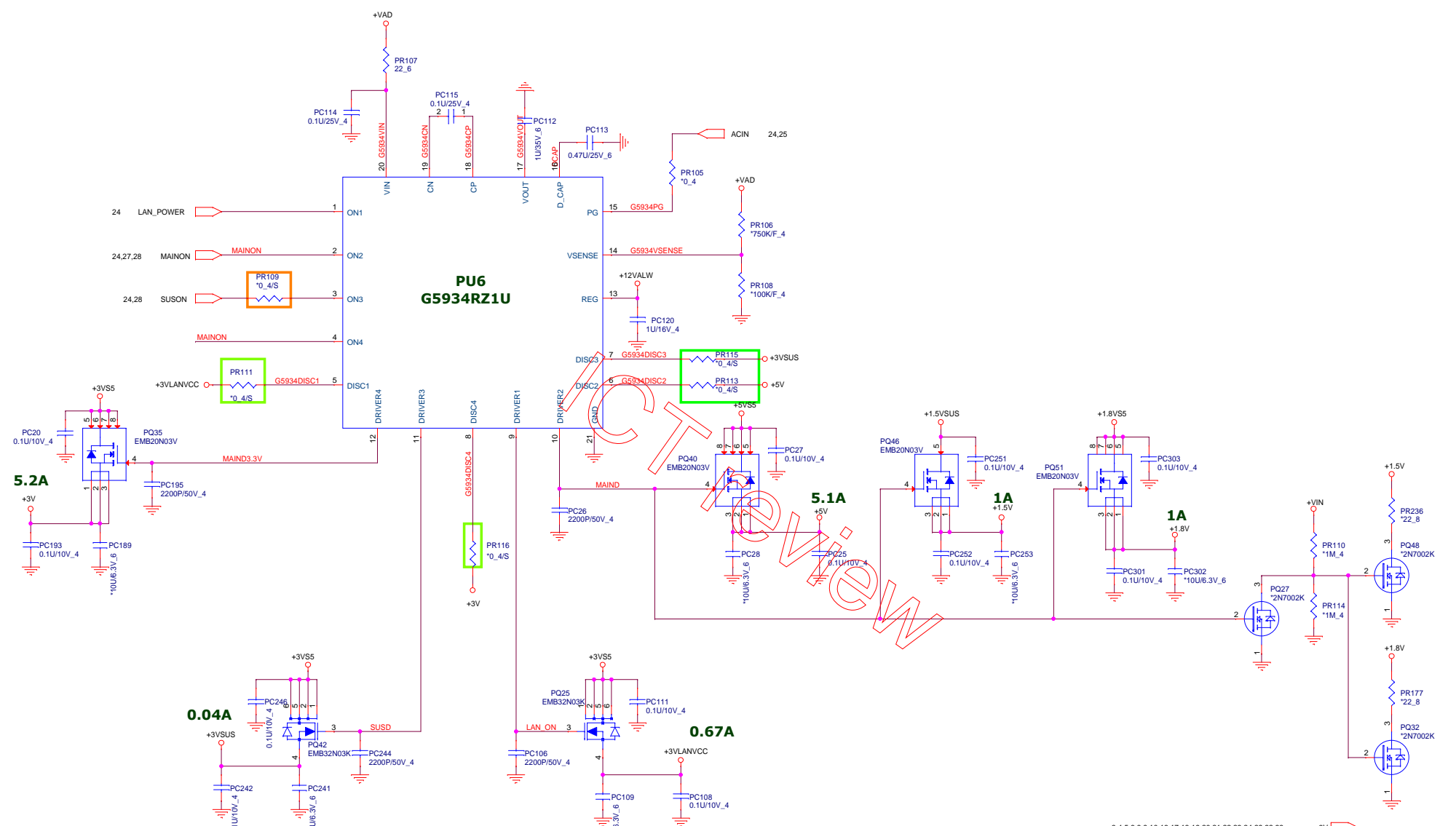
review

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Size Custom	Document Number DDR3 (TP551216)	Rev 1A
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 PROJECT :U99 Quanta Computer Inc.		

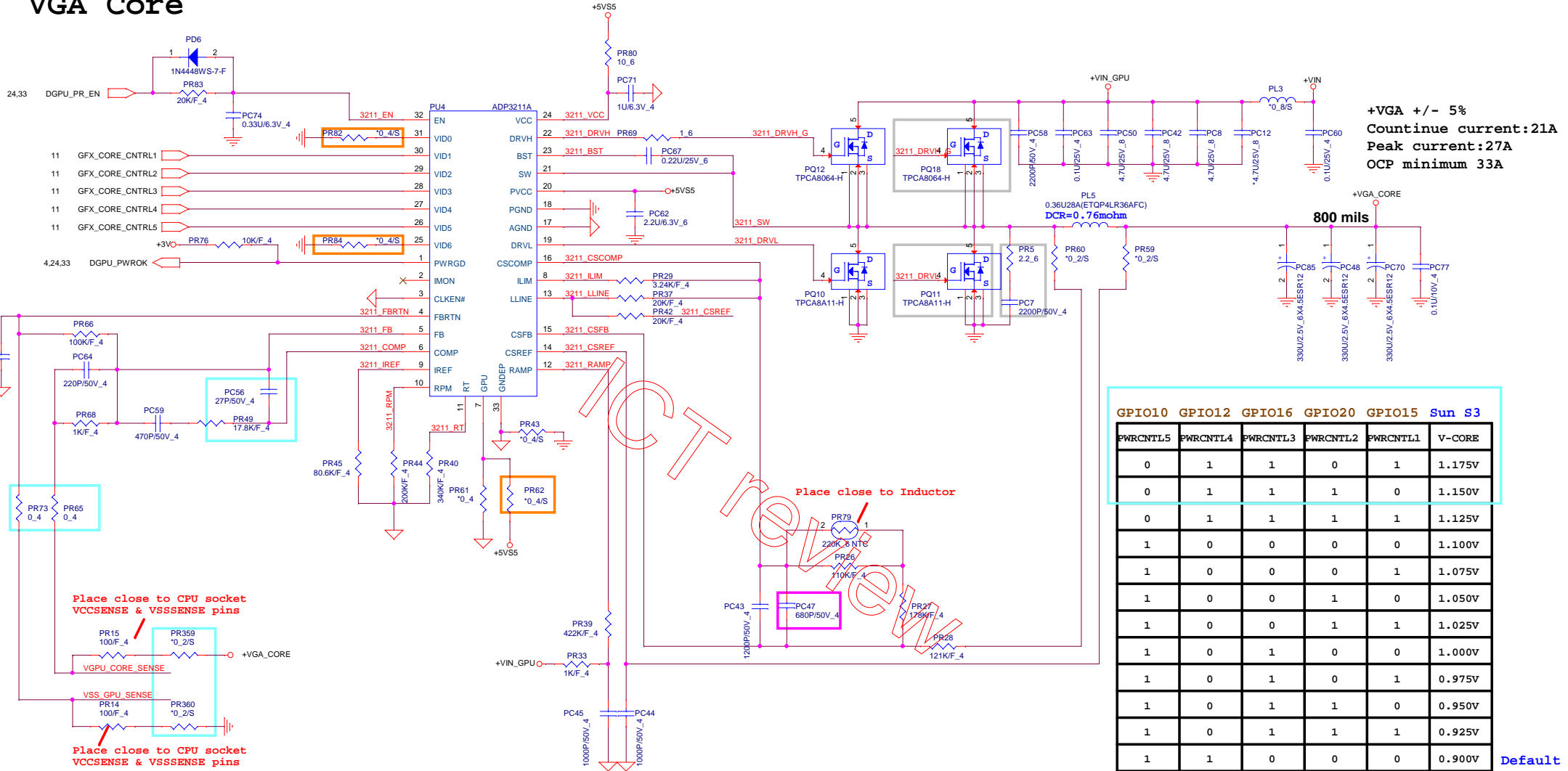




- 3,4,5,6,8,9,10,16,17,18,19,20,21,22,23,24,29,32,33 +3V
- 17,18,21,22 +5V
- 17,21,25,26,27,28,30,32,33 +VIN
- 4,5,6,7,23,24,26,27,33 +3VS5
- 18,22,26,27,28,29,30,32 +5VS5
- 25,33 +12VALW
- 19,23 +3VLANVCC
- 8,9,28 +0.75V_DDR_VTT

PROJECT :U99 Quanta Computer Inc.		
Size Custom	Document Number Dis-charge IC (SLG55448V)	Rev 1A
Date: Monday, May 19, 2014	Sheet 31	of 33

VGA Core



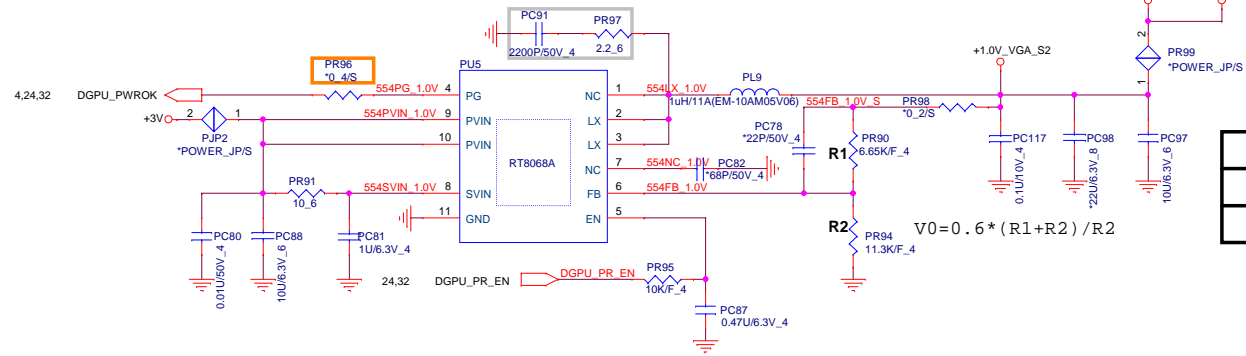
GPIO10	GPIO12	GPIO16	GPIO20	GPIO15	Sun S3	V-CORE
0	1	1	0	1	1.175V	
0	1	1	1	0	1.150V	
0	1	1	1	1	1.125V	
1	0	0	0	0	1.100V	
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	Default
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	
1	1	1	0	1	0.775V	

PROJECT :U99
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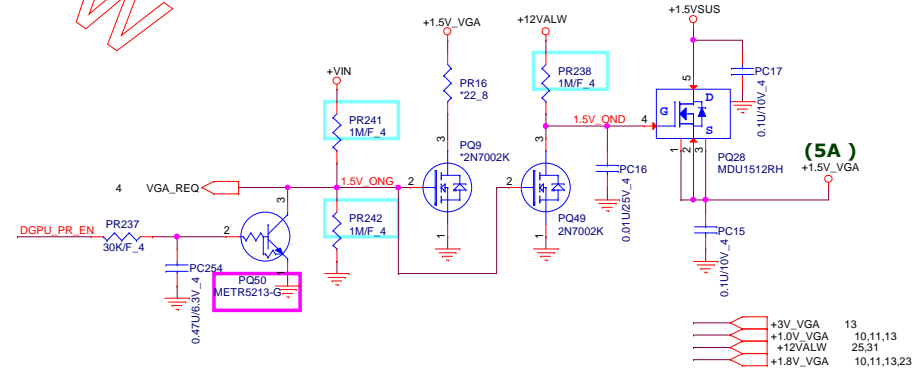
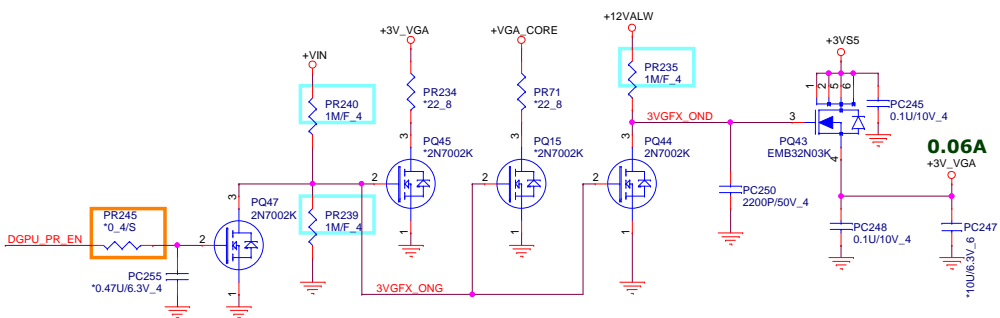
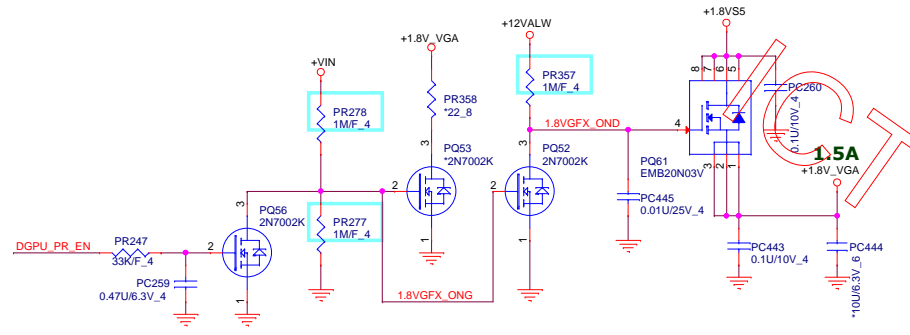
Size Custom Document Number +VGCORE NCP3218G Rev 1A

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+0.95V +/- 3%
Continue current:2A
Peak current:3A
OCP minimum:4A



R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V



- +3V_VGA 13
- +1.0V_VGA 10,11,13
- +12V_VALW 25,31
- +1.8V_VGA 10,11,13,23

DRAFT review

PROJECT :U99
Quanta Computer Inc.

Size Custom	Document Number +VGA POWER	Rev 1A
Date: Monday, May 19, 2014		Sheet 33 of 33