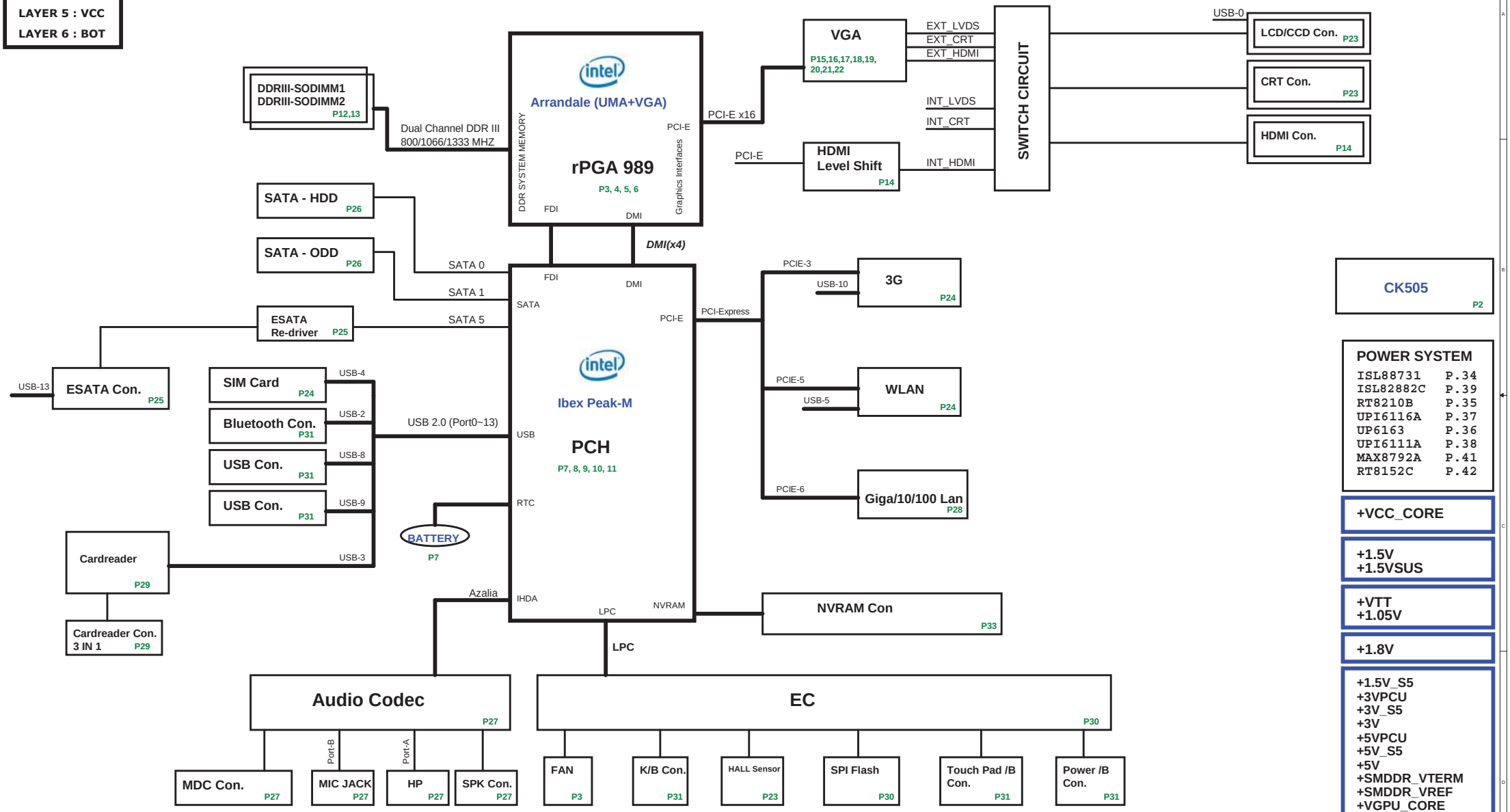
BL6 Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT



CK505 P2

POWER SYSTEM

ISL88731	P.34
ISL82882C	P.39
RT8210B	P.35
UPI6116A	P.37
UP6163	P.36
UPI6111A	P.38
MAX8792A	P.41
RT8152C	P.42

+VCC_CORE

+1.5V
+1.5VSUS

+VTT
+1.05V

+1.8V

+1.5V_S5
+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF
+VGPU_CORE
+VAXG

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PROJECT : BL6
Size | Document Number: Block Diagram | Rev: A1A
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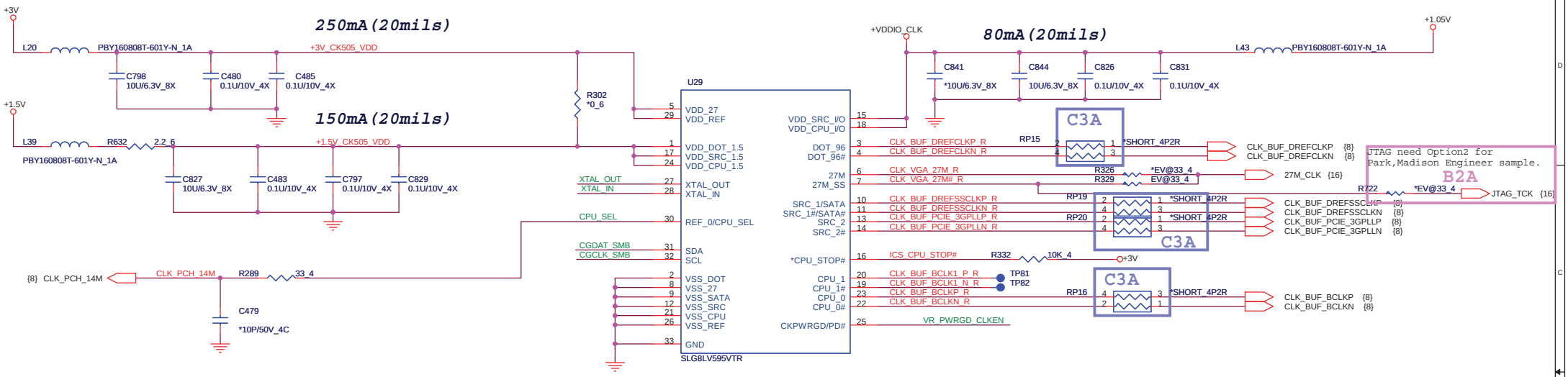
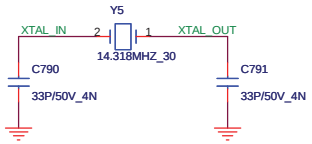
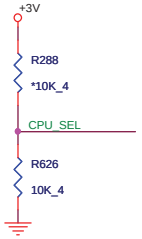
CLOCK Gen



CLK CRYSTAL

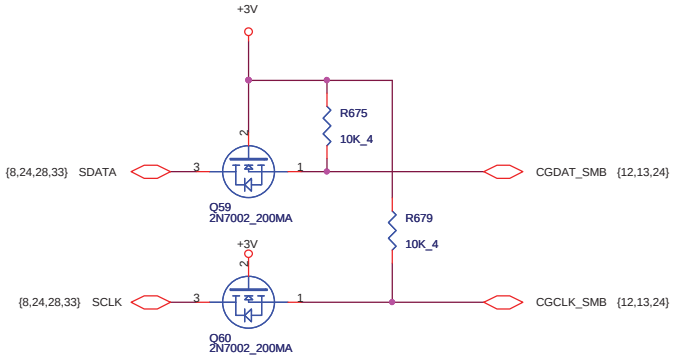


CLK CPU_SEL



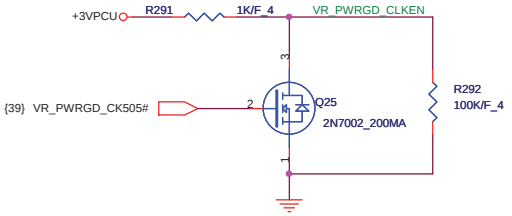
	0	1
CPU_SEL	CPU =133MHz (default)	CPU=100MHz

CLK I2C



CLK POWERGOOD

Change to +3VPCU
(follow CRB)



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PROJECT : BL6

Size	Document Number	Rev
	CLOCK GENERATOR	A1A
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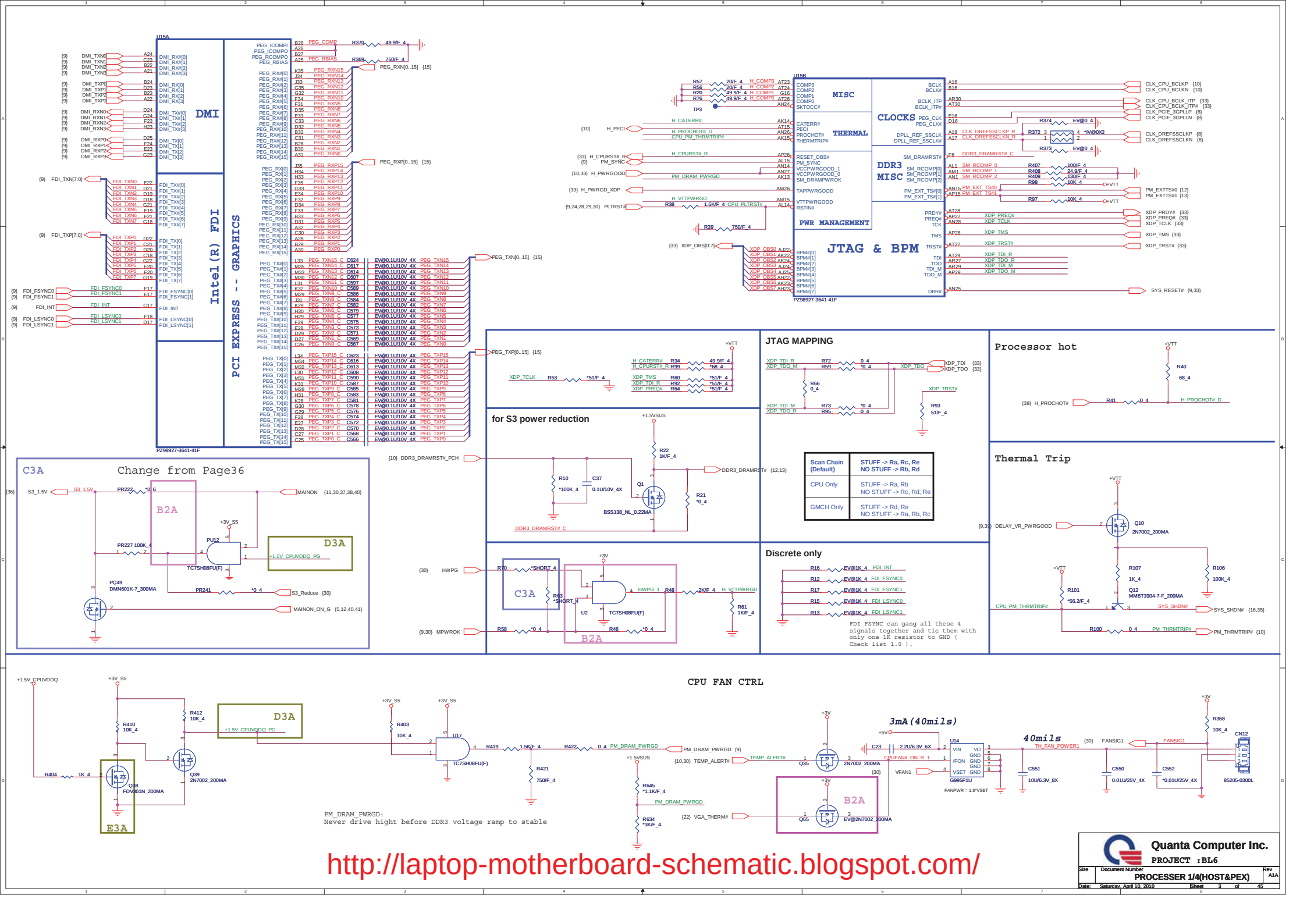

Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

PM_DRAM_PWRGD:
Never drive hight before DDR3 voltage ramp to stable

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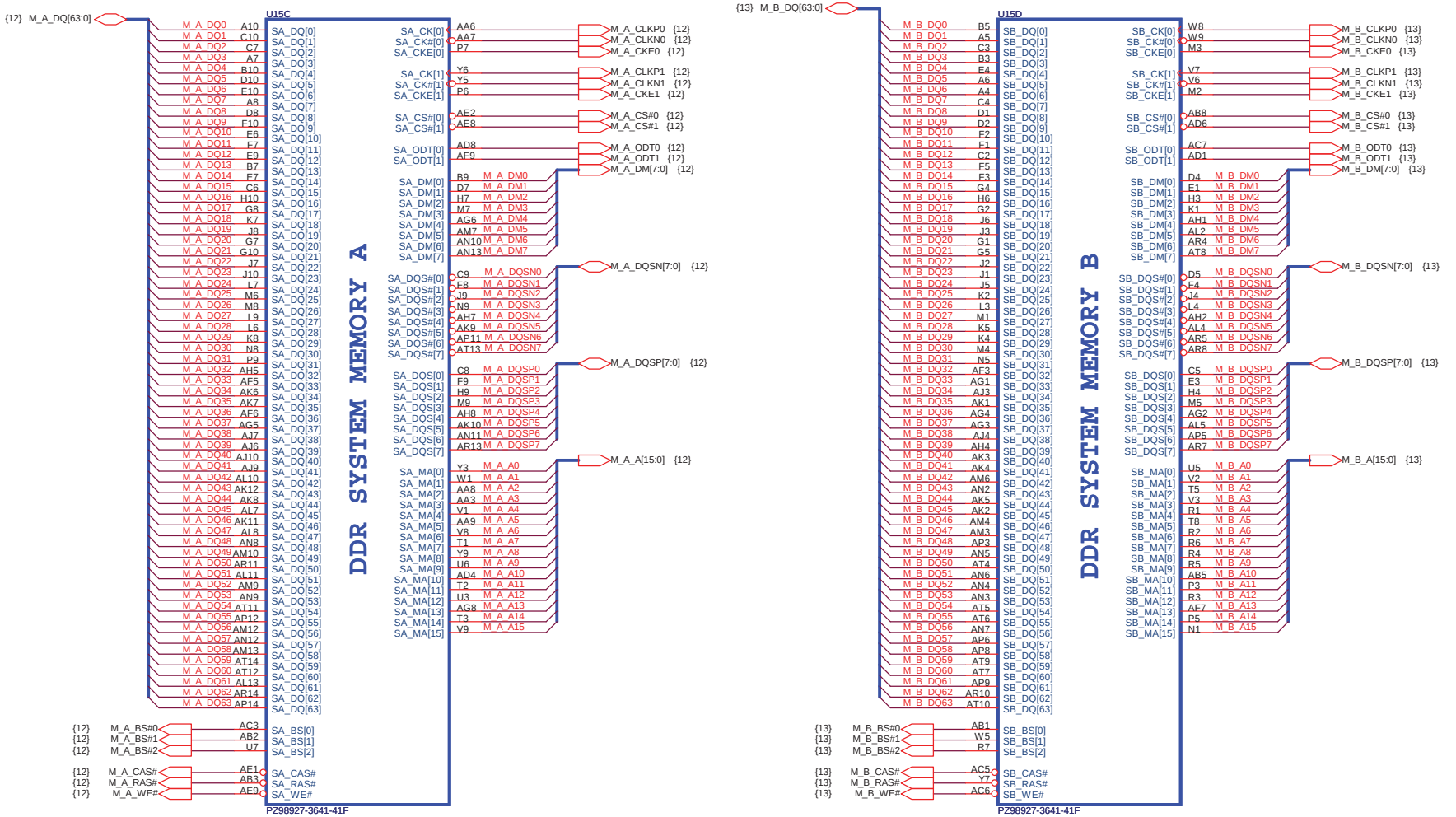
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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PROJECT : BL6

Size	Document Number	Rev
	PROCESSER 2/4(DDR)	A1A

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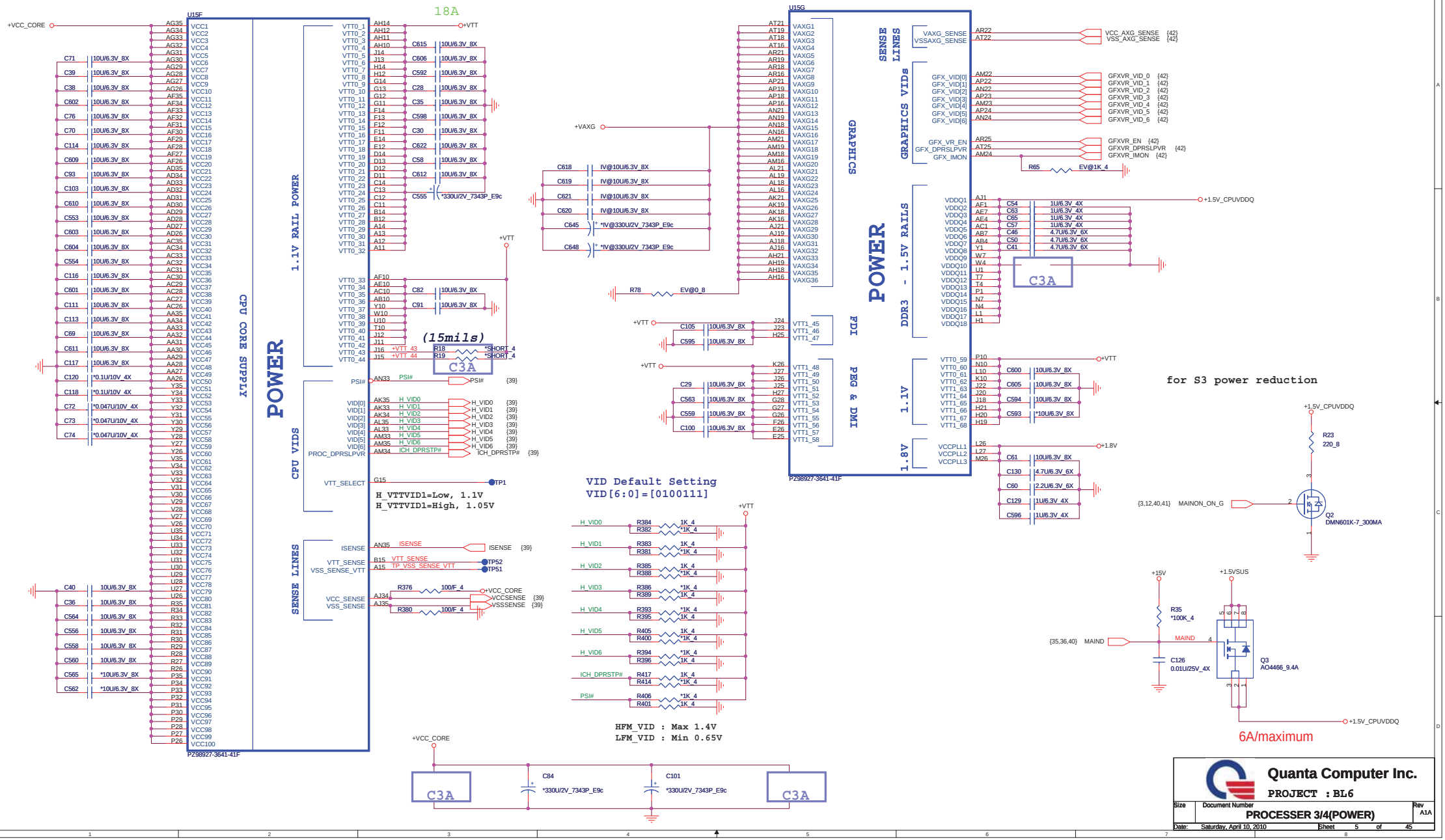

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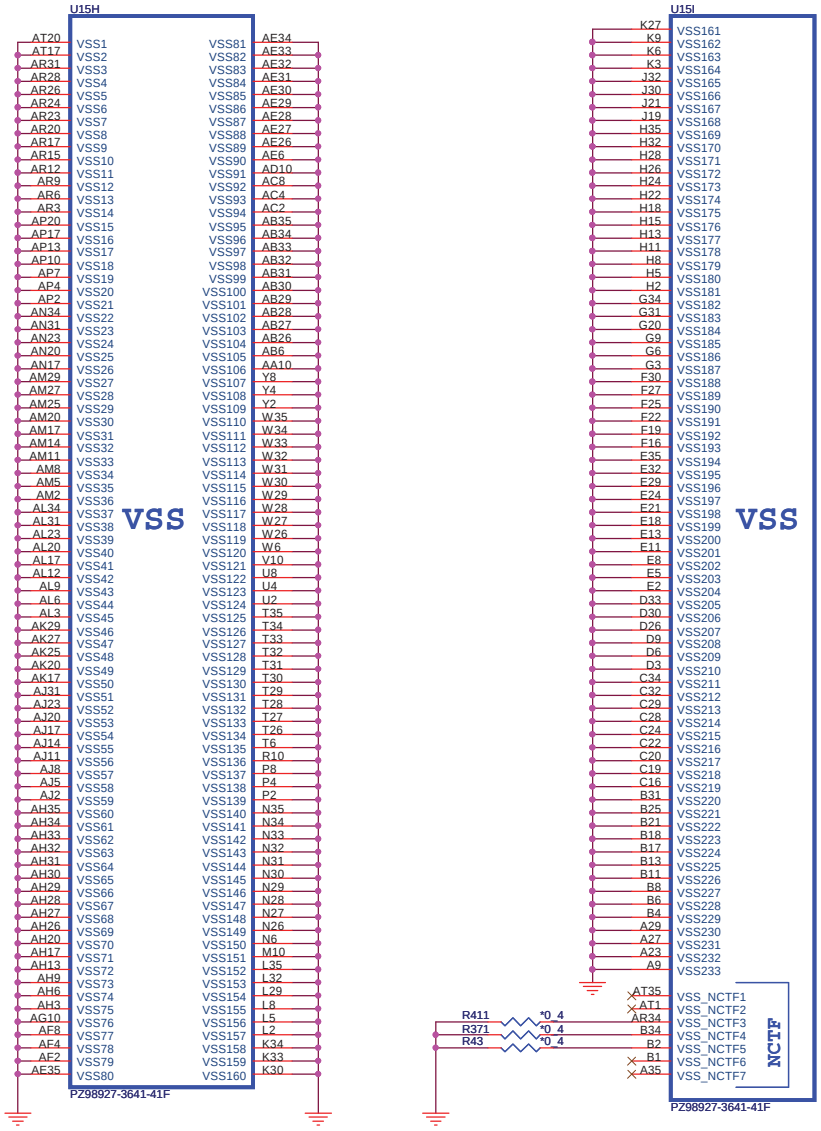
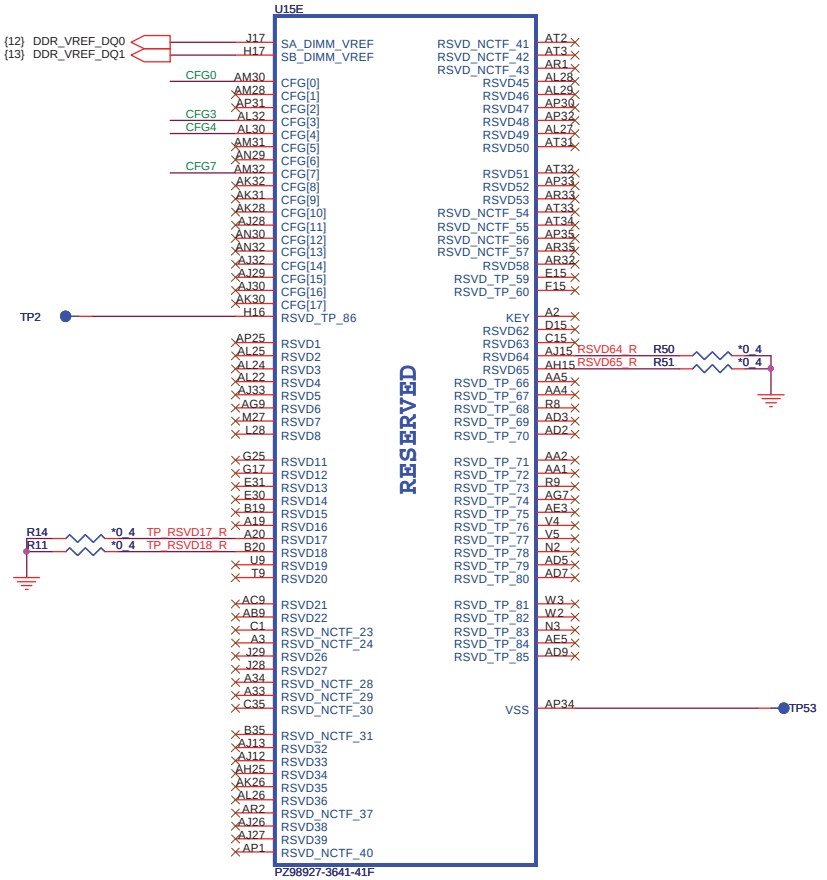
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Express Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

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Quanta Computer Inc.
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Size	Document Number	Rev
	PROCESSER 4/4 (GND)	1A

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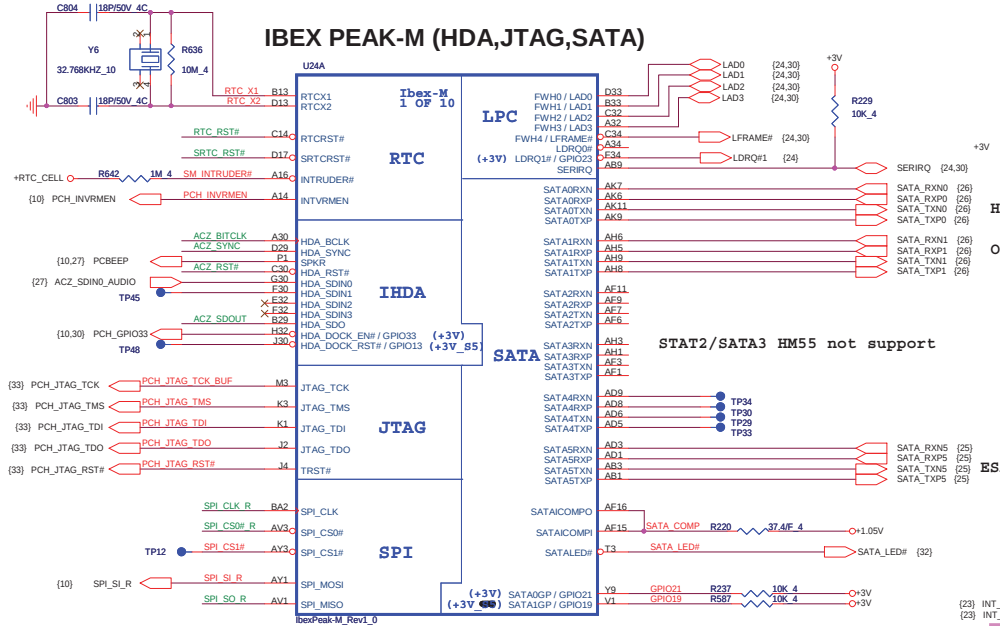
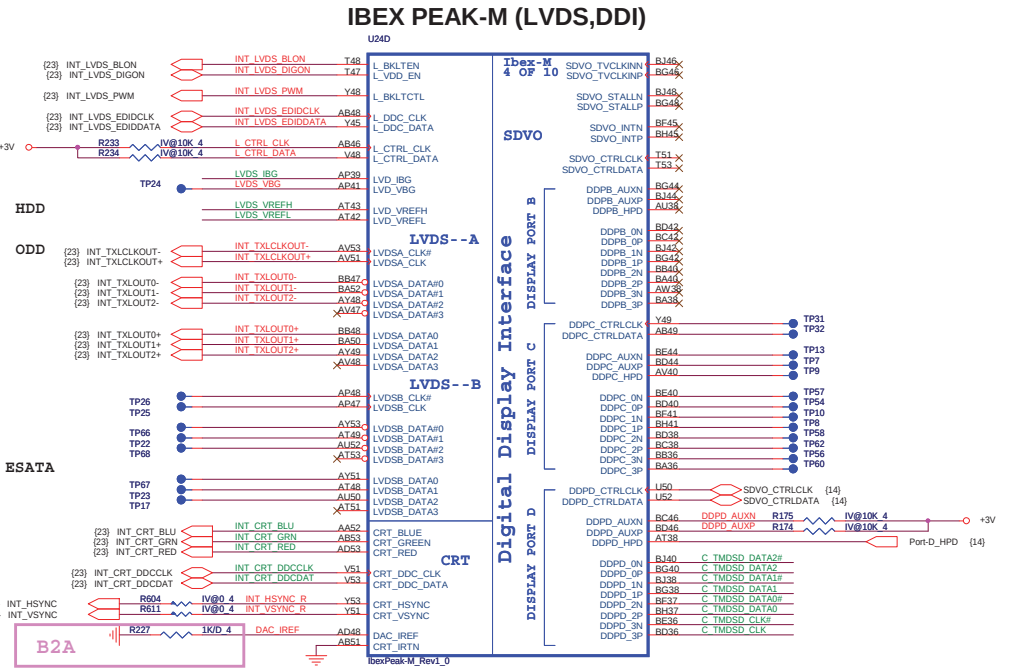
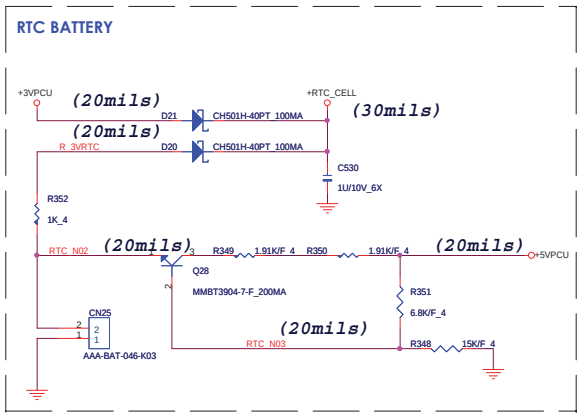
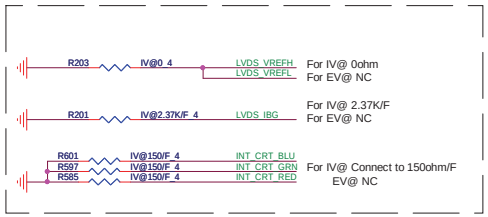
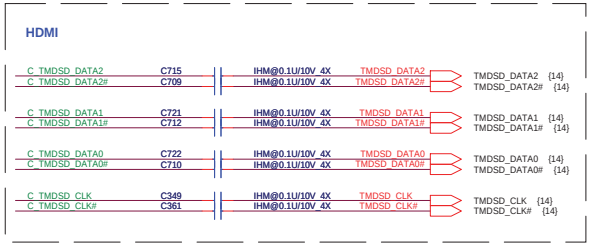


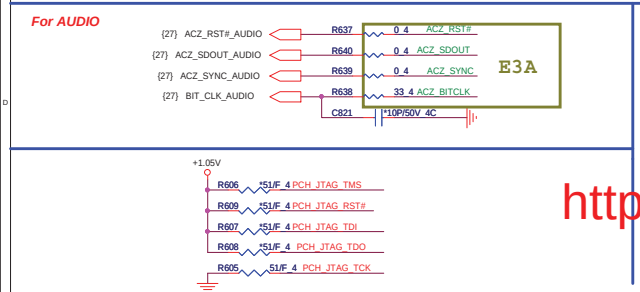


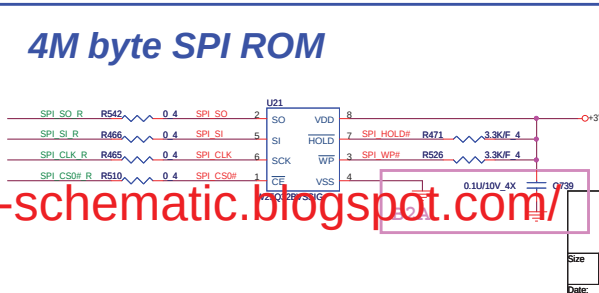
Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC











PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

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Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	A1A
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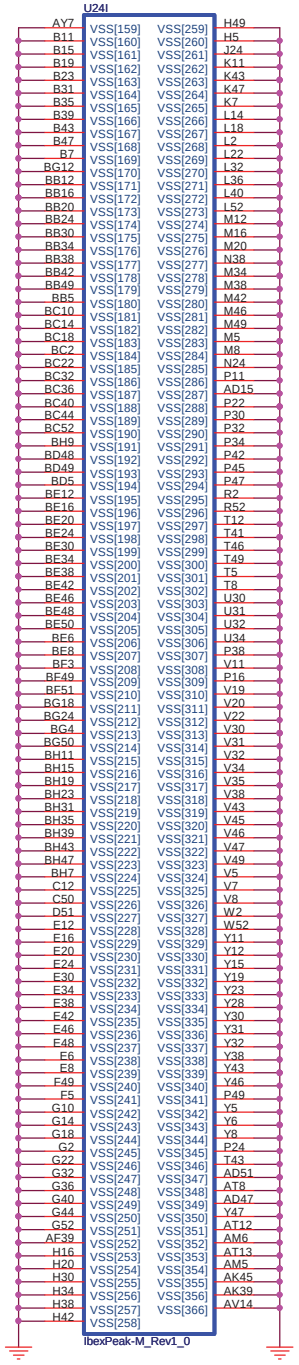
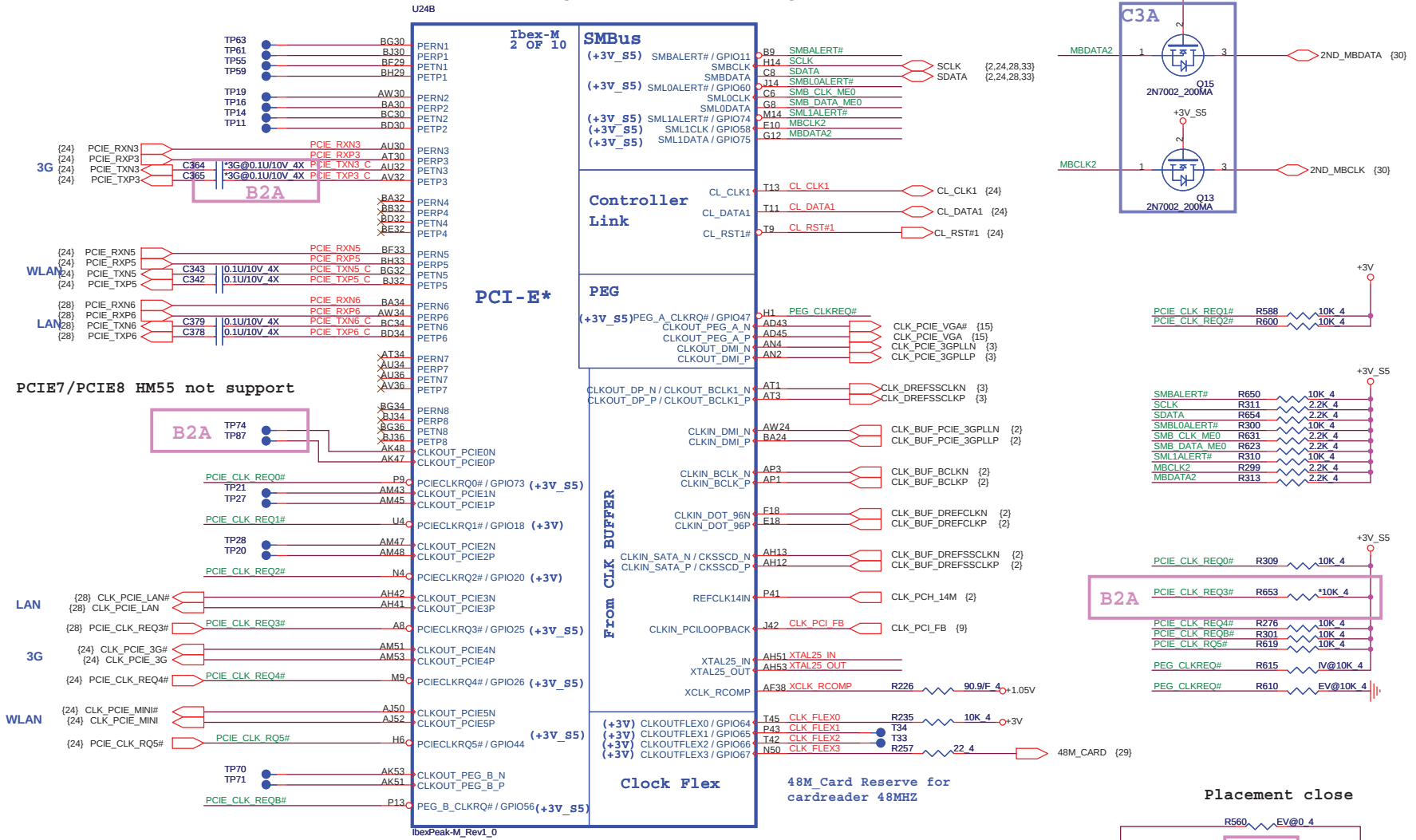
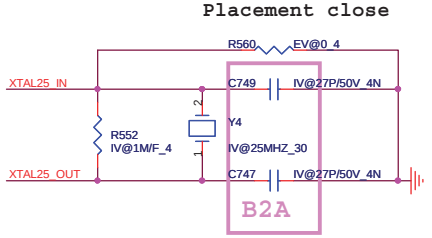
IBEX PEAK-M (GND)



IBEX PEAK-M (PCI-E,SMBUS,CLK)





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Size	Document Number	Rev
	PCH 2/5 (PCIE, SMBUS, CK)	A1A
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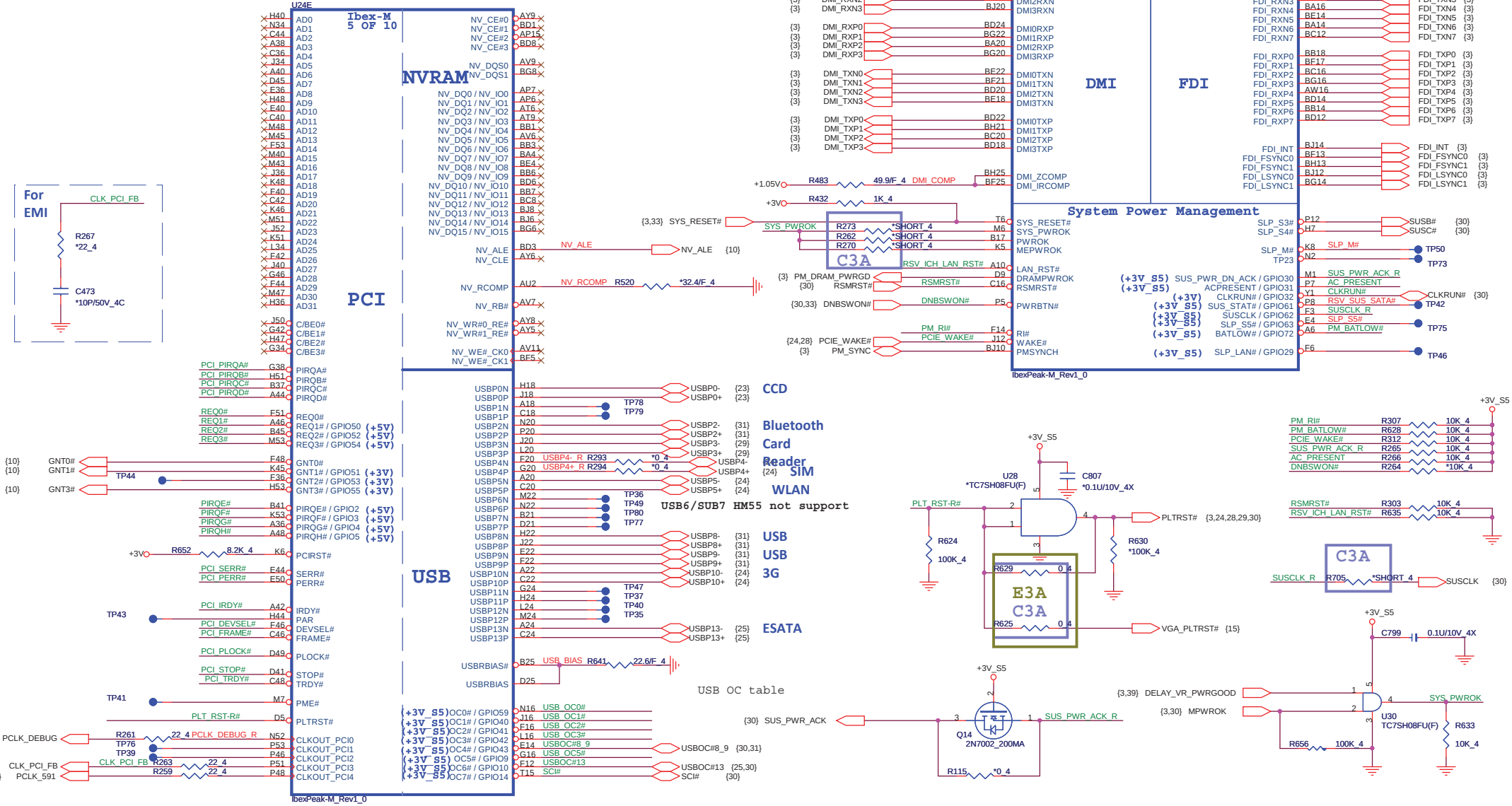
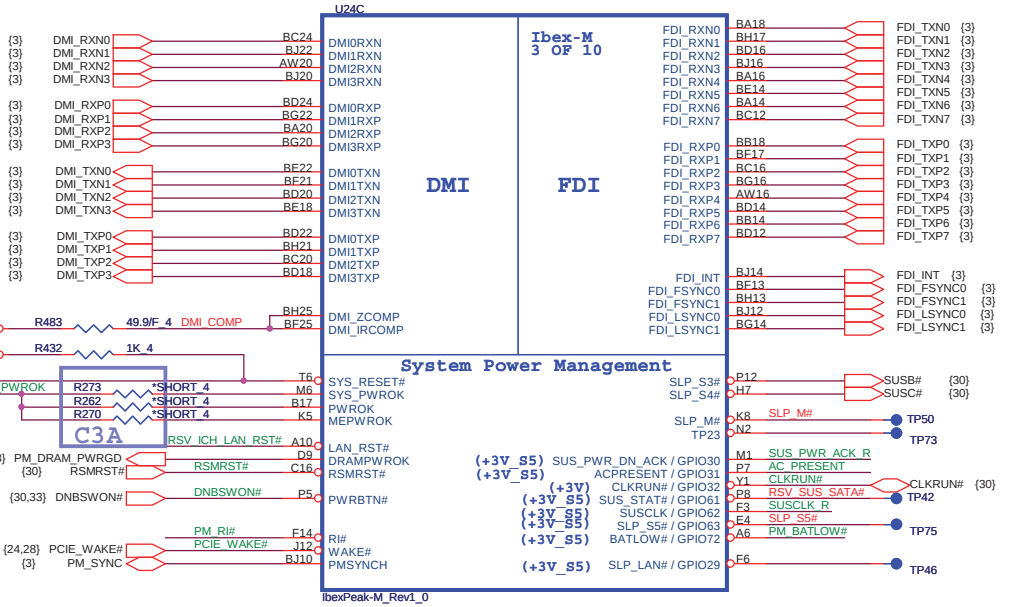
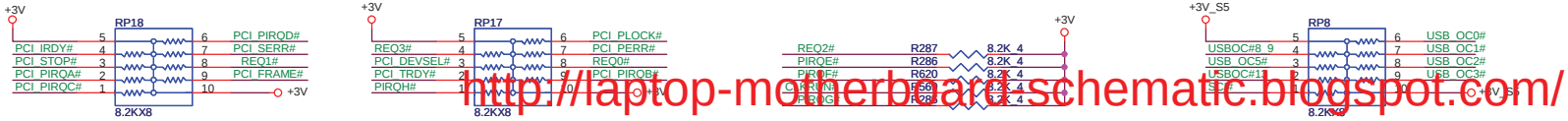
IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (DMI,FDI,GPIO)





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Quanta Computer Inc.
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Size	Document Number	Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)	A1A
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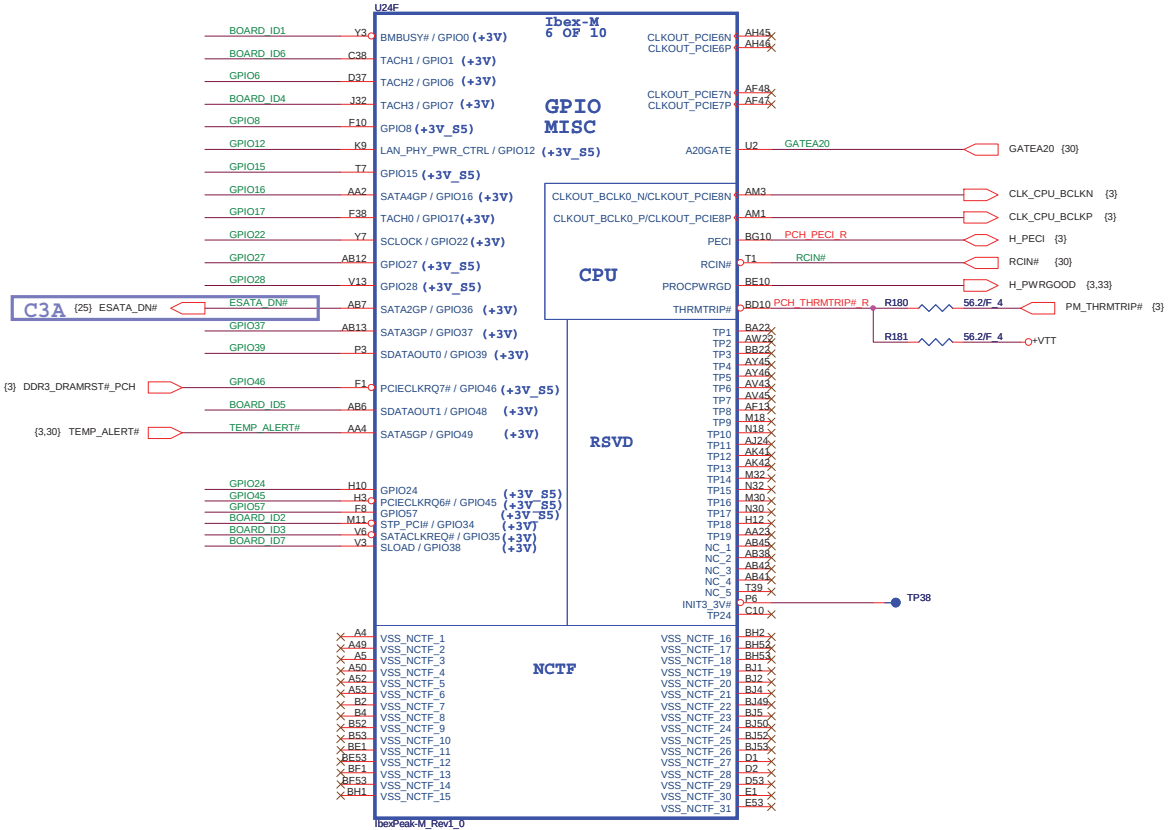
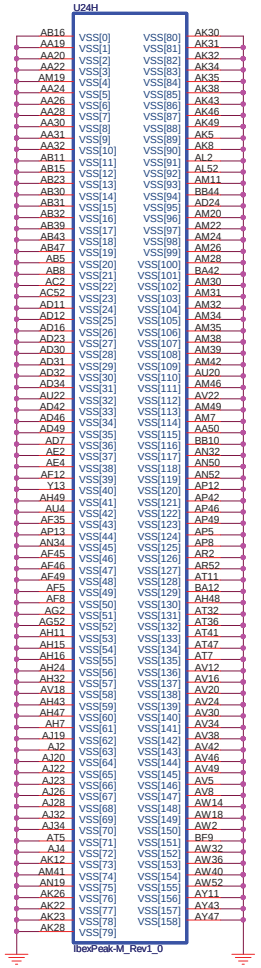
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



PCH Strap Pin Configuration Table

SPKR

{7,27} PCBEEP — R592 *1K_4 — +3V

Reboot option at power-up

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3#/ GPIO55

{9} GNT3# — R622 *10K_4

Top-Block Swap Override

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

HDA_DOCK_EN #/GPIO33

{7,30} PCH_GPIO33 — R282 1K_4 — E3A — JP1 *SHORT PAD

Flash Descriptor Security Override

0 = Flash Descriptor Security will be overridden
1 = Security measure defined in the Flash Descriptor will be enabled.

GNT0#, GNT1#

{9} GNT0# — R272 *1K_4
{9} GNT1# — R621 *1K_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

SPI_MOSI

{7} SPI_SI_R — R504 *1K_4 — +3V

TPM Functionality Disable

1 = Enabled
0 = Disable

NV_ALE

{9} NV_ALE — R496 *10K_4 — +1.8V

IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable

1 = Enabled
0 = Disabled (Default)

GPIO8

GPIO8 — R298 10K_4 — +3V_S5

Reserved

This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

GPIO15 — R248 1K_4 — +3V_S5

Reserved

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

GPIO27

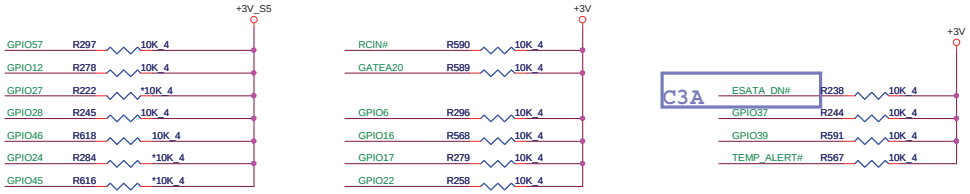
GPIO27 — R232 *10K_4

On-Die PLL Voltage Regulator

0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
This signal has a weak internal pull-up.

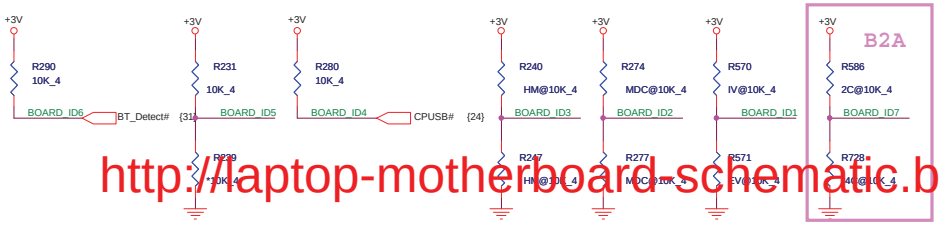
+RTC_CELL — R644 330K_6 — PCH_INVRMEN — {7}

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs



BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7
UMA SKU VGA SKU	H L						
W/ MDC W/O MDC		H L					
W/ HDMI W/O HDMI			H L				
W/O 3G W/ 3G				H L			
15" 14"					H L		
W/O BT W/ BT						H L	
2 Core 4 Core							H L



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Quanta Computer Inc.
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Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	A1A
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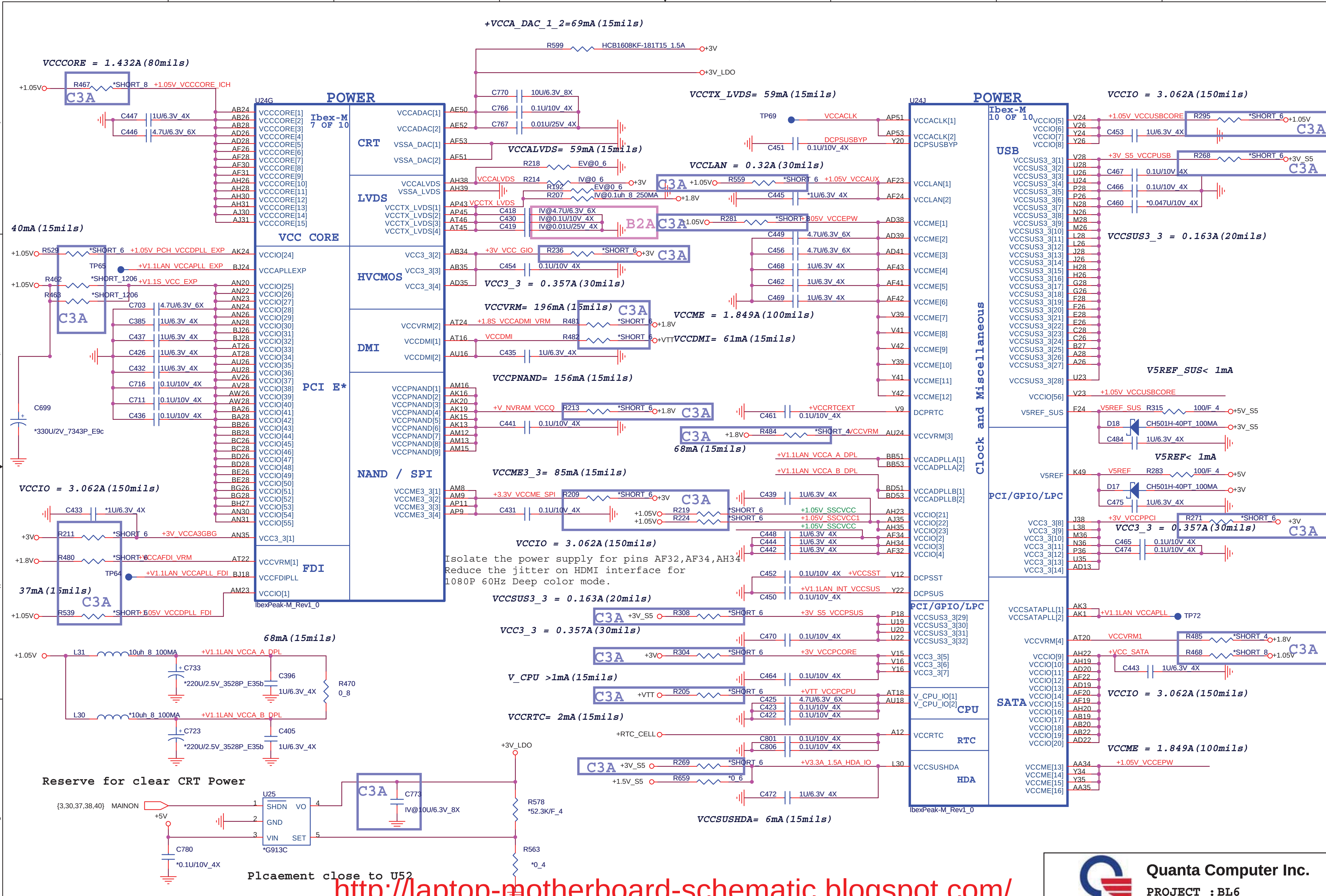

POWER
U24G
Ibex-M 7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
IbexPeak-M_Rev1_0
POWER
U24J
Ibex-M 10 OF 10
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IbexPeak-M_Rev1_0
+VCCA_DAC_1_2=69mA(15mils)
VCCCORE = 1.432A(80mils)
VCCTX_LVDS= 59mA(15mils)
VCCIO = 3.062A(150mils)
VCCALVDS= 59mA(15mils)
VCCLAN = 0.32A(30mils)
40mA(15mils)
VCCSUS3_3 = 0.163A(20mils)
VCC3_3 = 0.357A(30mils)
VCCVRM= 196mA(15mils)
VCCME = 1.849A(100mils)
VCCDMI= 61mA(15mils)
VCCPNAND= 156mA(15mils)
V5REF_SUS< 1mA
68mA(15mils)
V5REF< 1mA
VCCME3_3= 85mA(15mils)
VCCIO = 3.062A(150mils)
VCC3_3 = 0.357A(30mils)
VCCIO = 3.062A(150mils)
Isolate the power supply for pins AF32,AF34,AH34
Reduce the jitter on HDMI interface for
1080P 60Hz Deep color mode.
37mA(15mils)
VCCSUS3_3 = 0.163A(20mils)
68mA(15mils)
VCC3_3 = 0.357A(30mils)
V_CPU >1mA(15mils)
VCCIO = 3.062A(150mils)
VCCRTC= 2mA(15mils)
VCCME = 1.849A(100mils)
Reserve for clear CRT Power
VCCSUSHDA= 6mA(15mils)
Plcaement close to U52
U25
*G913C
C3A
B2A

Quanta Computer Inc.

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	PCH 5/5 (POWER)	A1A

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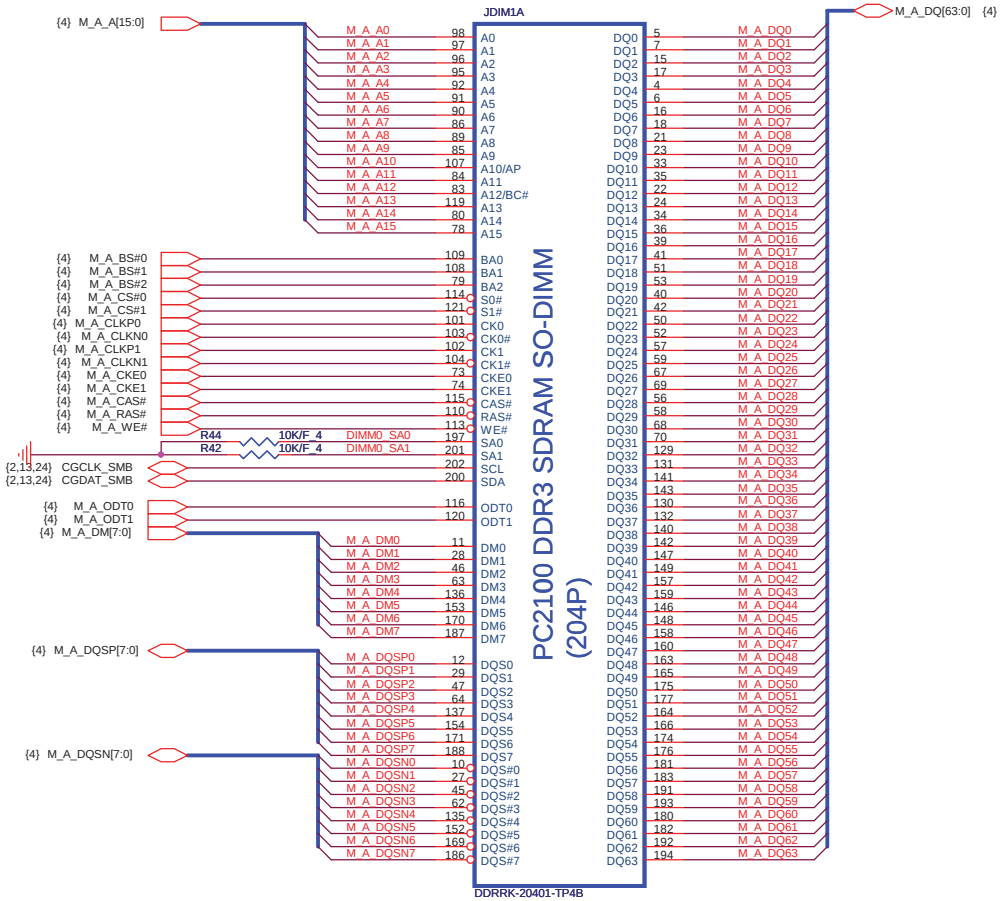
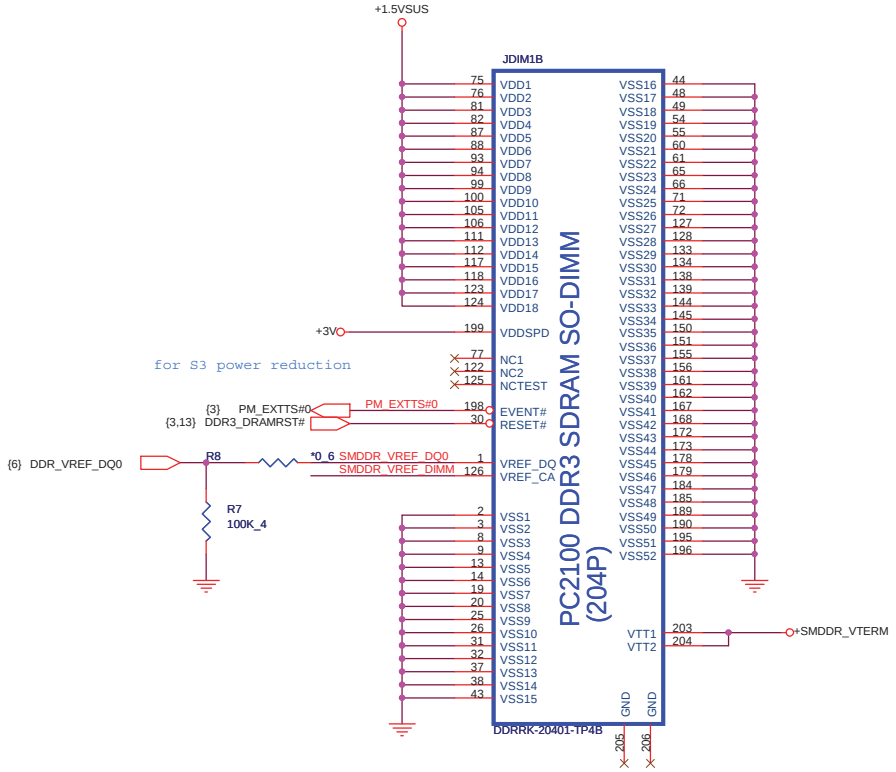
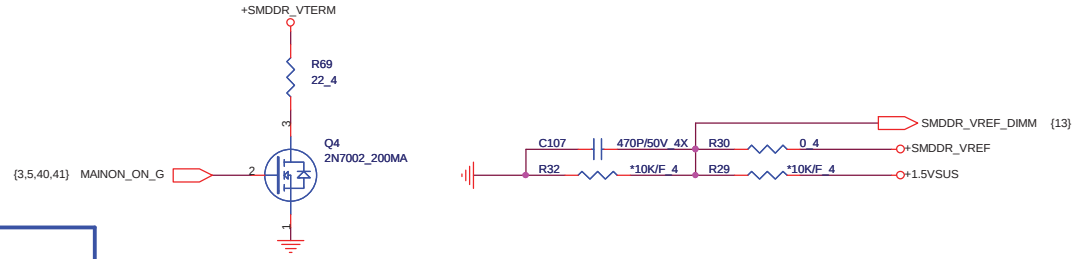
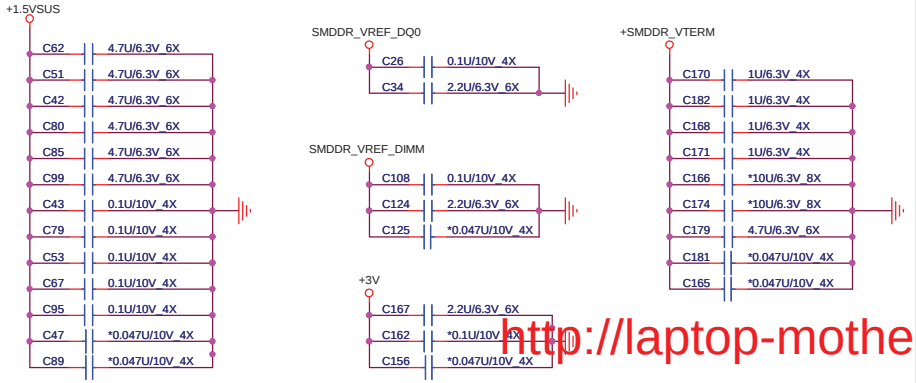
H=4

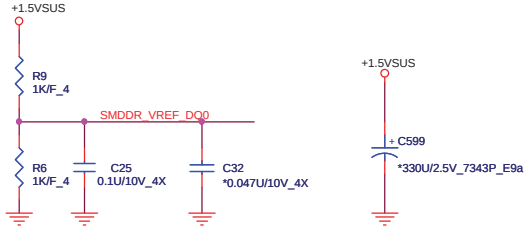






Place these Caps near So-Dimm0.





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	DDR3 DIMM-0	A1A
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H=8

JDIM2A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP8D

H=8

JDIM2B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP8D

Place these Caps near So-Dimm1.

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Size	Document Number	Rev
	DDR3 DIMM-1	A1A

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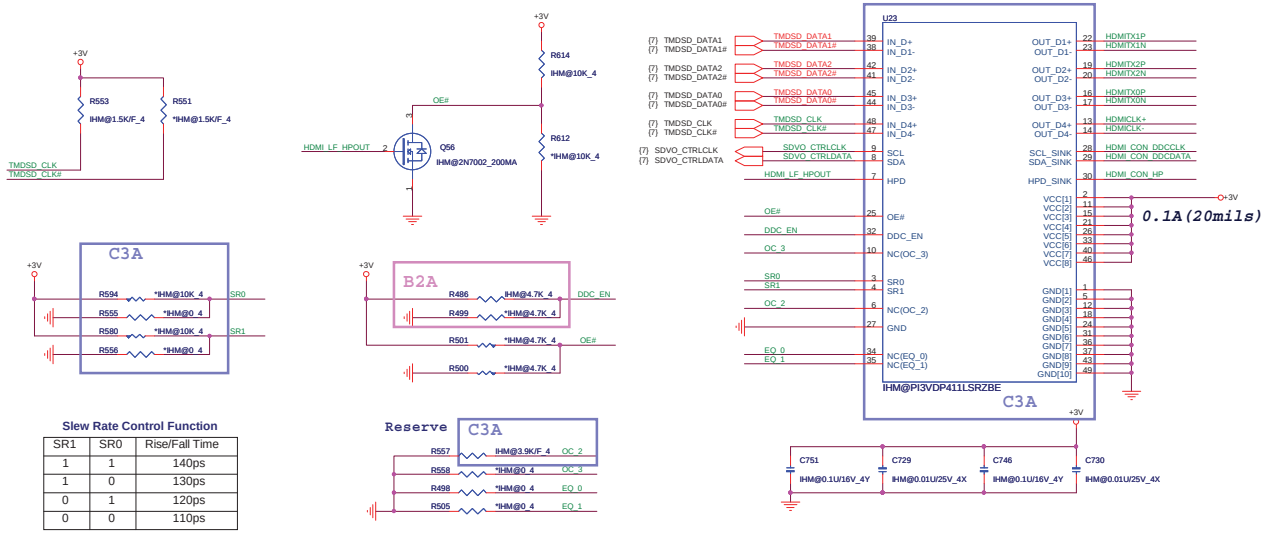
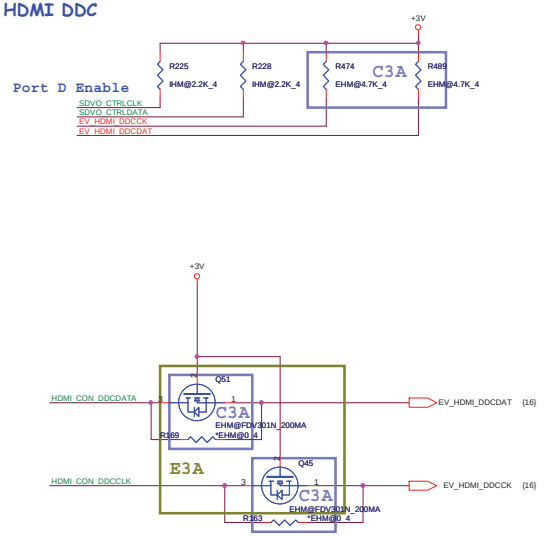
HDMI Level Shift



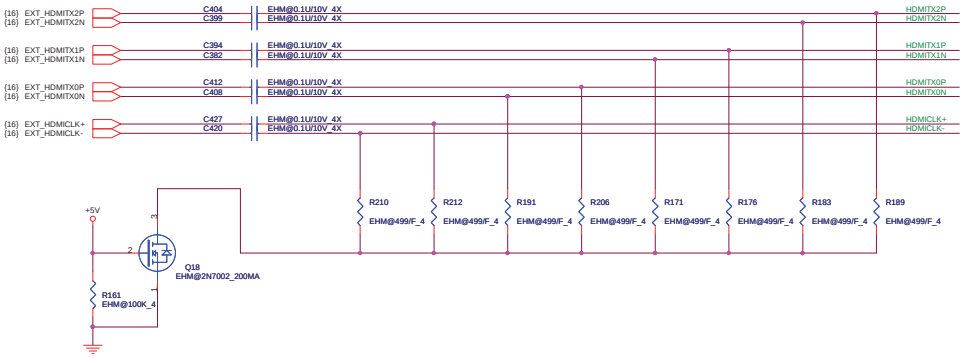
Slew Rate Control Function

SR1	SR0	Rise/Fall Time
1	1	140ps
1	0	130ps
0	1	120ps
0	0	110ps

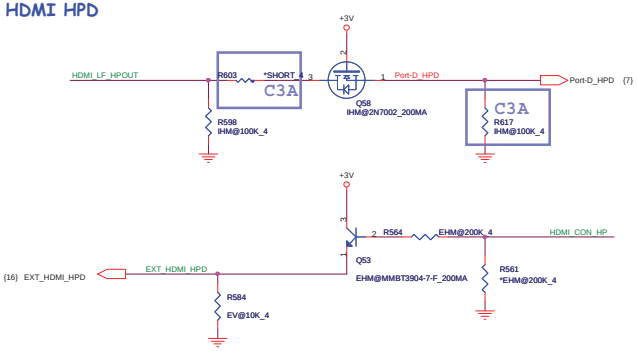
HDMI DDC



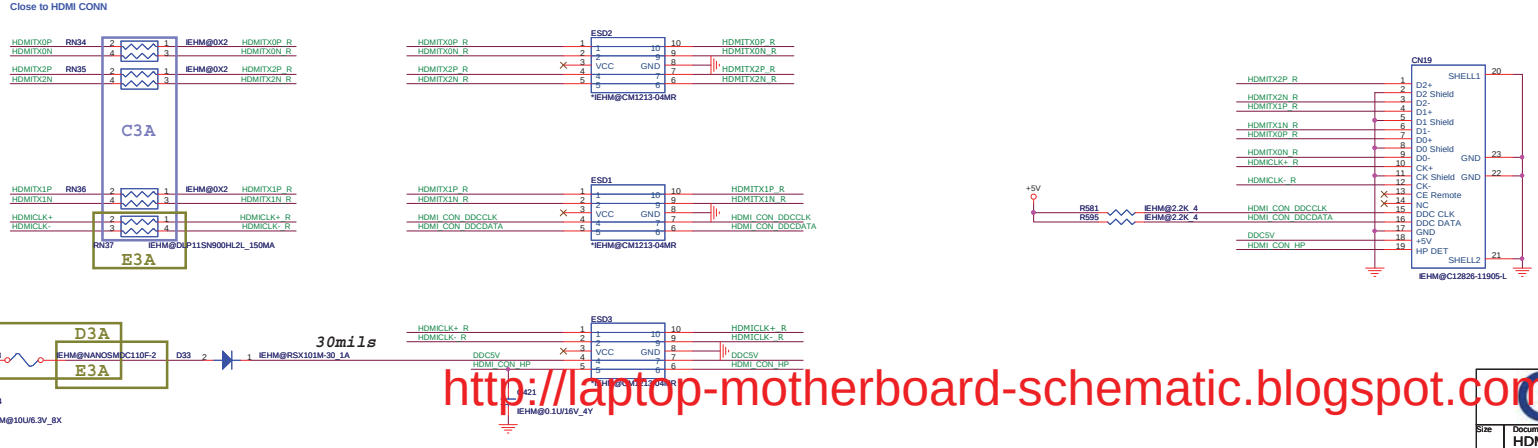
Discrete HDMI



HDMI HPD



Close to HDMI CONN



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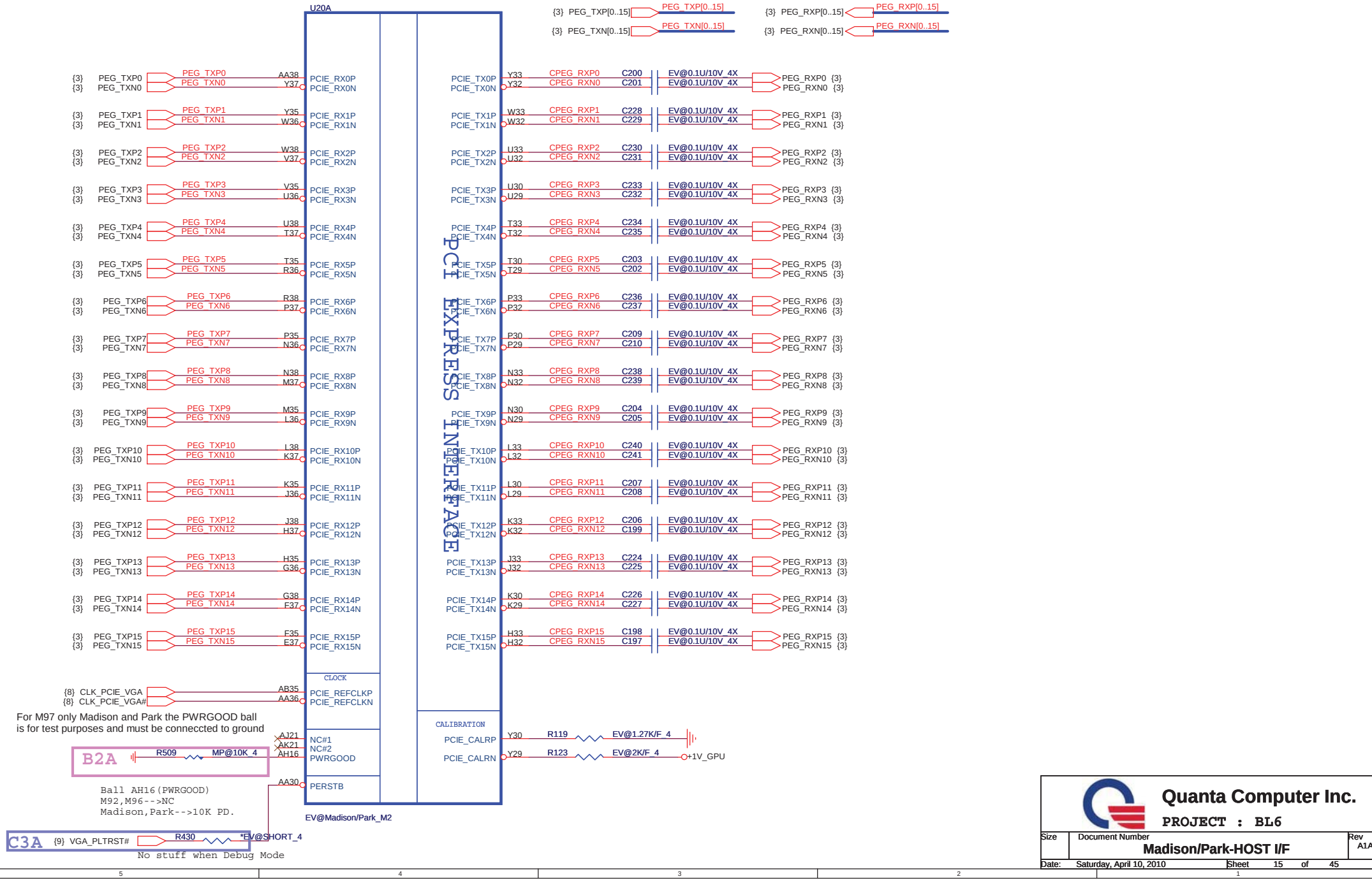
Quanta Computer Inc.
PROJECT : BL6
Size | Document Number: HDMI CONN | Rev: A1A
Date: Saturday, April 10, 2010 | Sheet 14 of 45



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B2A

JTAG SIGNAL STUFF OPTION FOR OPTION2

SIGNALS	NORMAL MODE	JTAG MODE (DEBU
TESTEN	"1" (PU)	"1" (PU)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)

1.8V GPIO

B2A
NC on Park
M92,M96,Madison support

B2A
NC on Park
M92,M96,Madison support

SCL must be tied high if not used

B2A
Park Channel D-->No support
M92 Channel C&D-->No support

HDMI

LVDS

EV@Madison/Park_M2

TjMax = 110
change by VBIOS

B2A
M92,M96 GPIO_21 pin control BB function.Park,Madison no suport.

B2A
M96,Madison-->support Ball AH26-->HPD5 Ball AH24-->HPD6 M92,Park-->No support

JTAG need Option2 for Park,Madison Engineer sample

Place close to Chip

+1.8V(20mA)

5mA (5mils)

(3.3V@130mA A2VDD)

(1.8V@70mA AVDD)

(1.8V@45mA VDD1DI/ 50mA VFF2D)

(1.8V@1.5mA A2VDDQ)

B2A
Madison,Park-->22mA (10mil)
M92,M96-->30mA (20mil)

B2A
Port 3
M96,Madison,Park-->support
M92-->No support
Port 4
M96,Madison-->support
M92,Park-->No support

CRT

B2A
Port7
Madison-->support
M92,M96,Park-->No support

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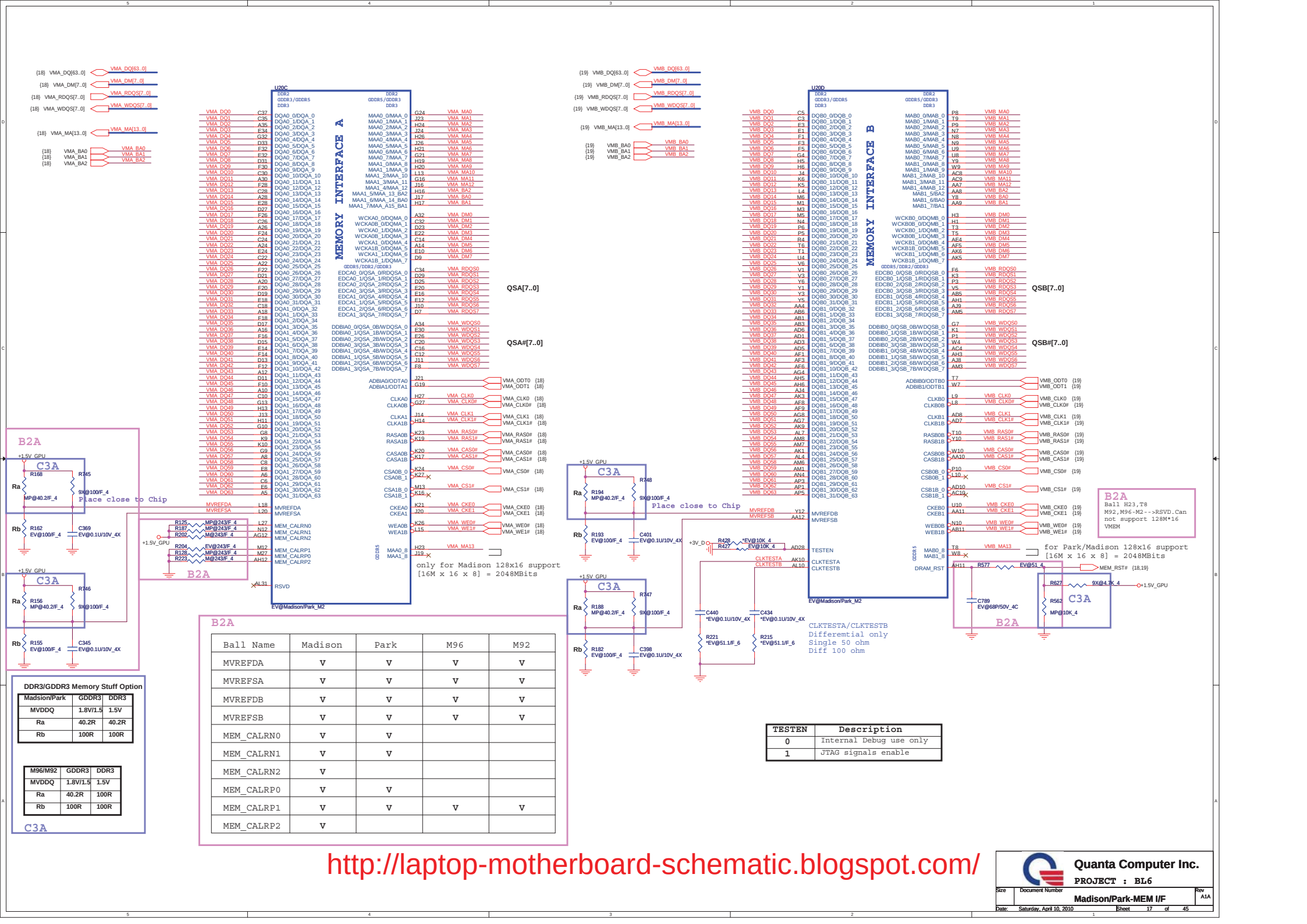

DDR3/GDDR3 Memory Stuff Option

Madsion/Park	GDDR3	DDR3
MVDDQ	1.8V/1.5	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

M96/M92	GDDR3	DDR3
MVDDQ	1.8V/1.5	1.5V
Ra	40.2R	100R
Rb	100R	100R

C3A

Ball Name	Madison	Park	M96	M92
MVREFDA	V	V	V	V
MVREFSA	V	V	V	V
MVREFDB	V	V	V	V
MVREFSB	V	V	V	V
MEM_CALRN0	V	V		
MEM_CALRN1	V	V		
MEM_CALRN2	V			
MEM_CALRP0	V	V		
MEM_CALRP1	V	V	V	V
MEM_CALRP2	V			

TESTEN	Description
0	Internal Debug use only
1	JTAG signals enable

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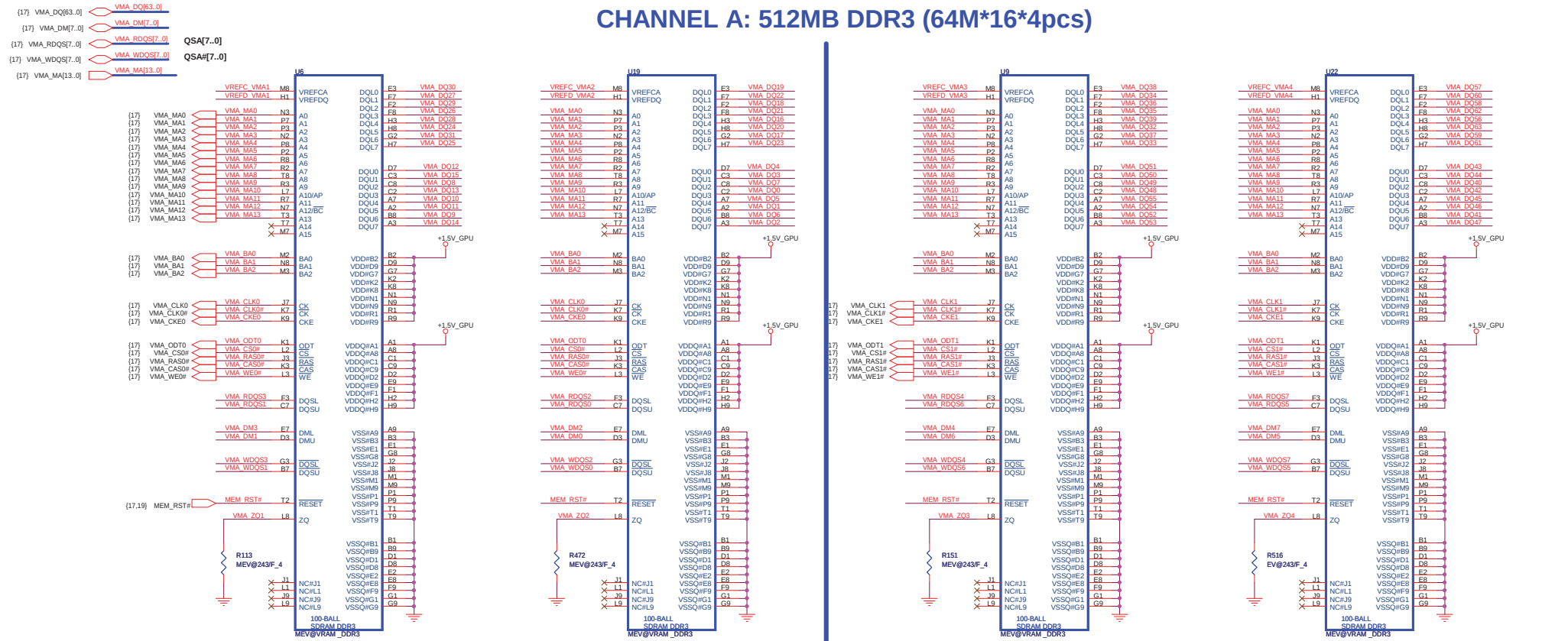
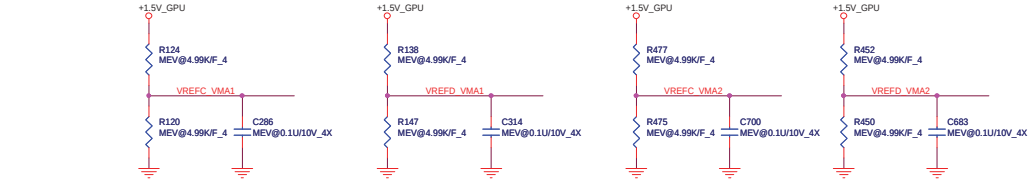
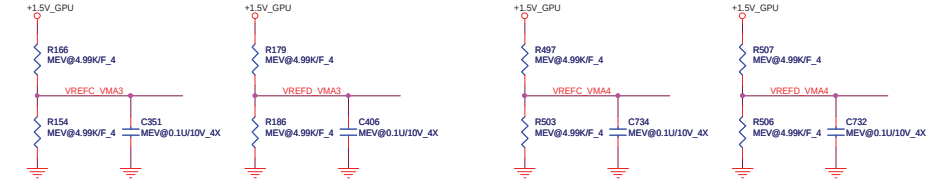
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



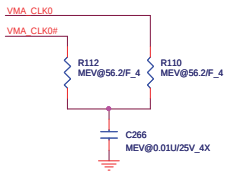
Group-A0 VREF



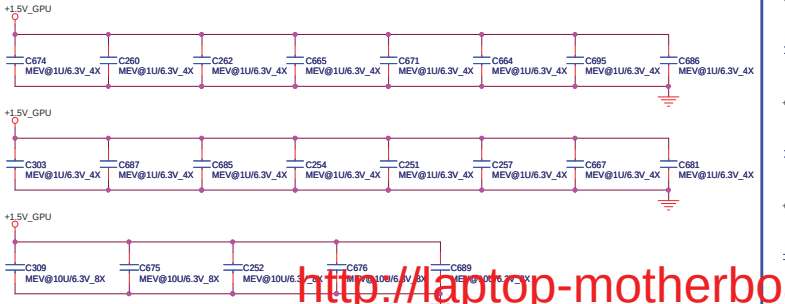
Group-A1 VREF



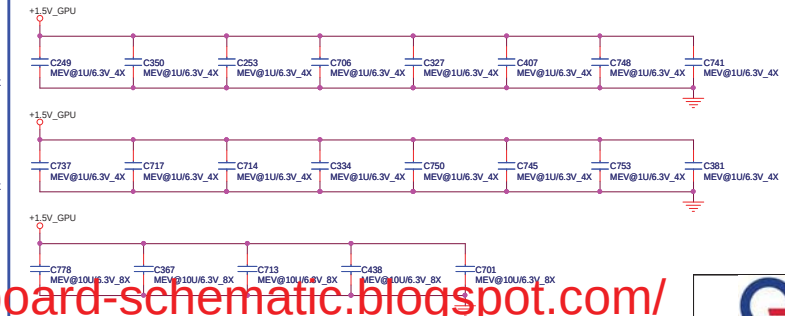
MEM_A0 CLK



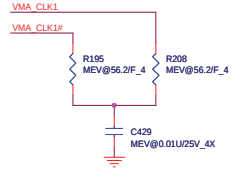
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



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	VRAM_A: DDR3-64M*16*4PCS	A1A

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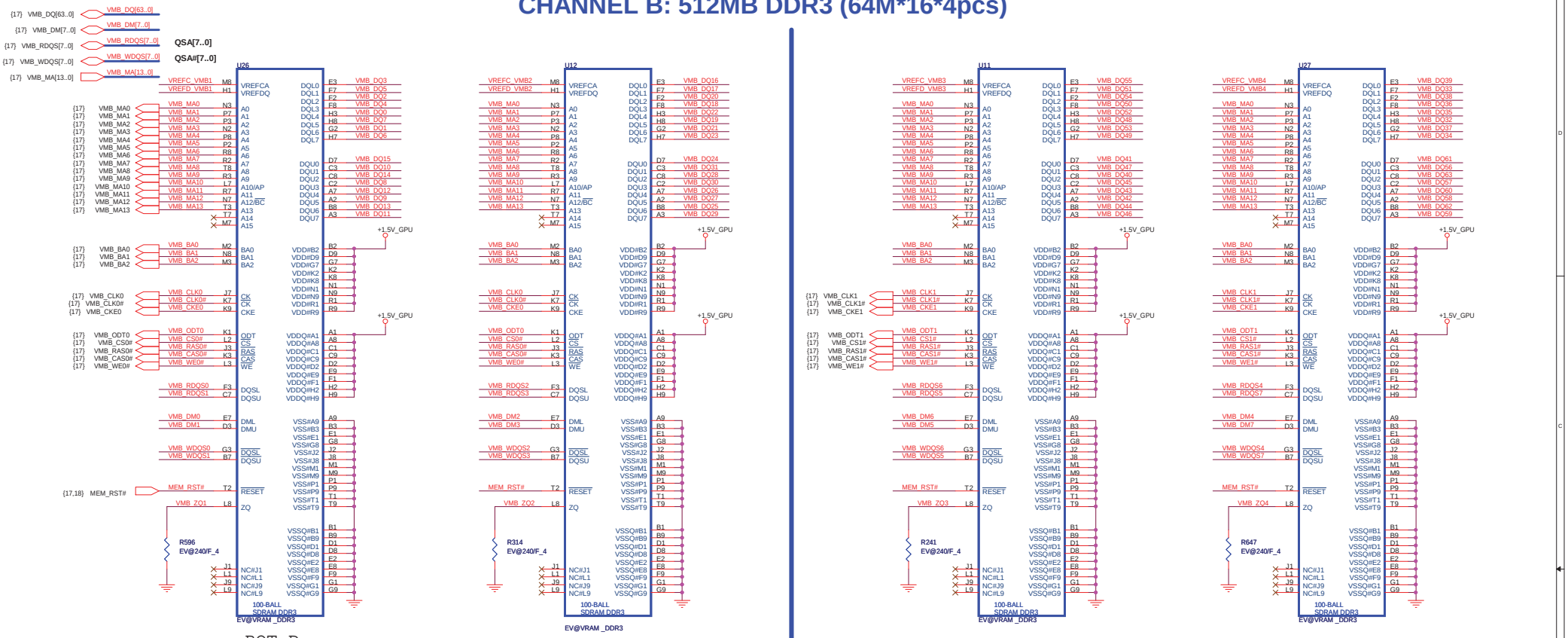
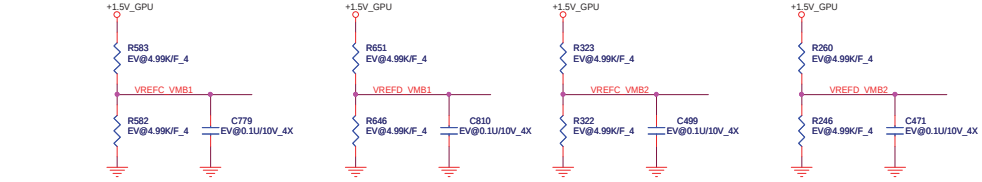
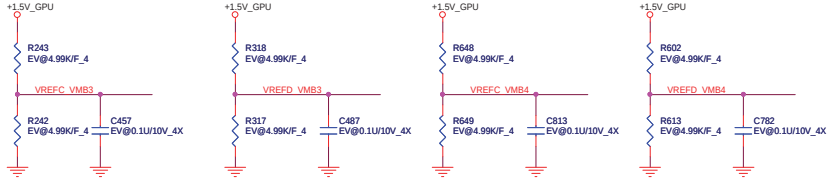
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



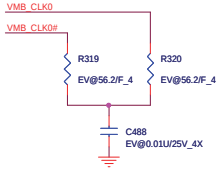
Group-B0 VREF



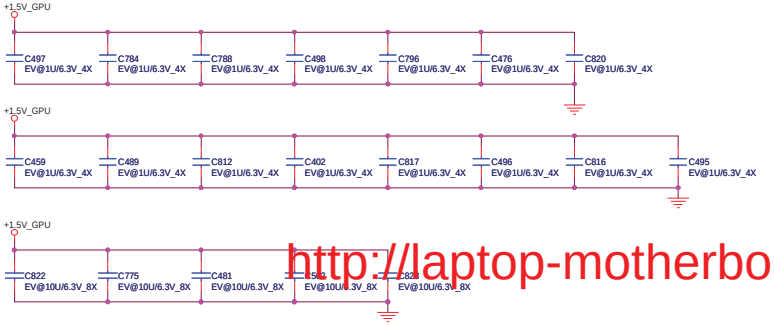
Group-B1 VREF



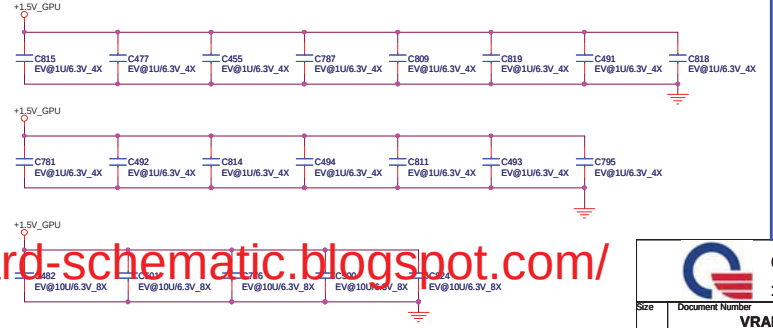
MEM_B0 CLK



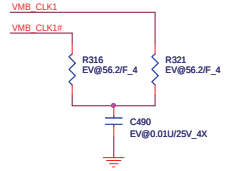
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



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Size	Document Number	Rev
	VRAM_B: DDR3-64M*16*4PCS	A1A
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For Madison and Park VDDCI and VDDC can share one common regulator

VDD/VDDQ =1.5V at 1333
VDD/VDDQ =1.8V at 1600 and 1800

(1.5V@3.4A_VDDR1)

(1.8V@400mA PCIE_VDDR)

(1.0V@2A PCIE_VDDC)

(1.8V@17mA VDD_CT)

(3.3V@60mA)

(1.8V@170mA)

(1.8V@40mA PCIE_PVDD)

(1.8V@150mA MPV18)

(1.8V@50mA SPV18)

(1.0V@100mA SPV10)

(30A or more)

(DDR3 1.12V@4A VDDCI) or more

VDDCI:33.6A

GND

POWER

Route as differential Pair

GPU +3V power
0.5A

PowerXpress control signal for Madsion and Park only
If not used, can be disconnected. (AL21 pin)

PX_EN = LOW, turn on
PX_EN = HIGH, turn off

	M92	M96	Park	Madison
VDDRHA	NC	VDDR1	NC	NC
VDDRHB	VDDR1	VDDR1	NC	NC
VSSRHA	NC	VSS	NC	NC
VSSRHB	VSS	VSS	NC	NC

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Size: Document Number: Madison/Park PWR_GND Rev: A1A
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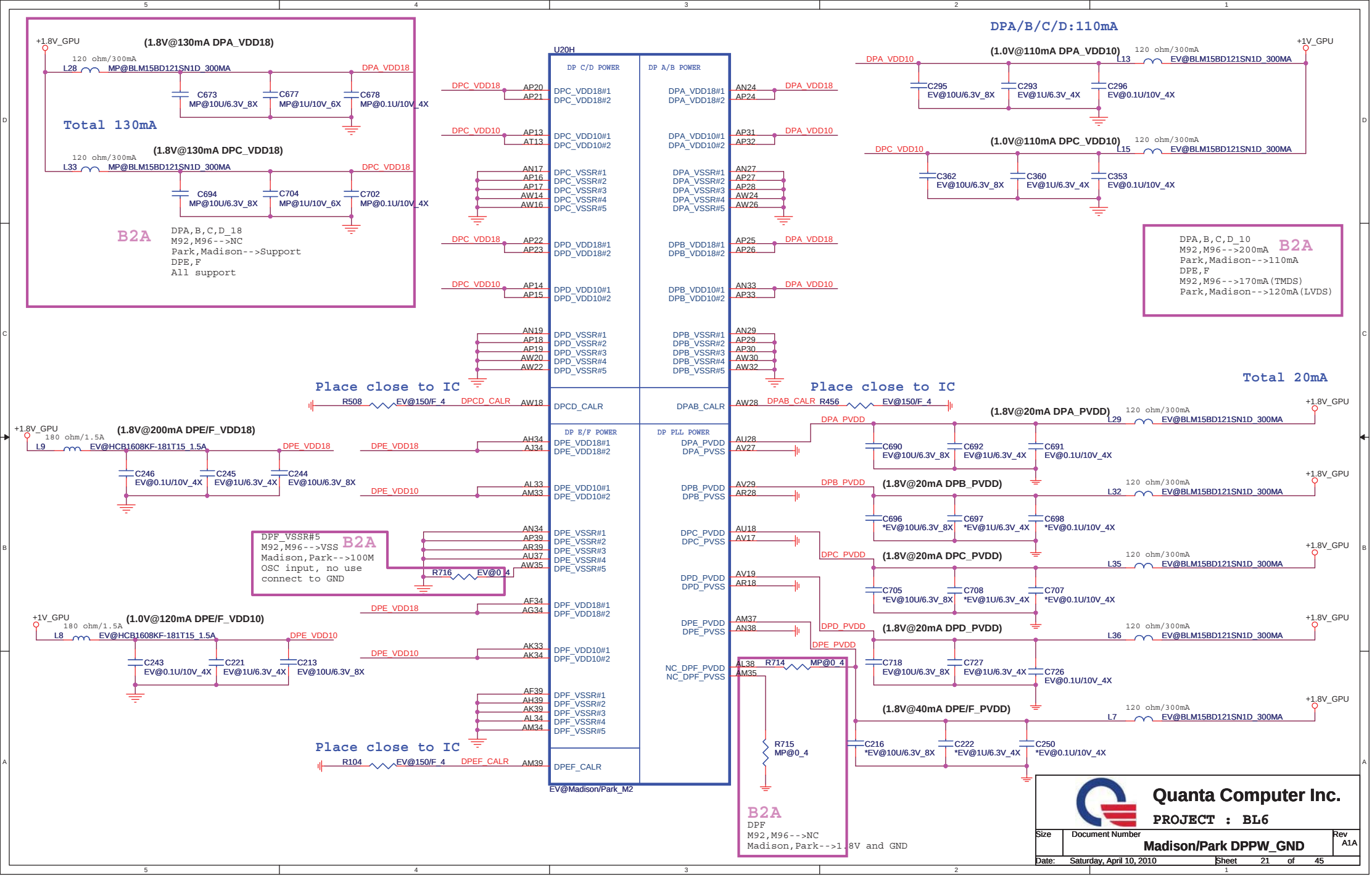

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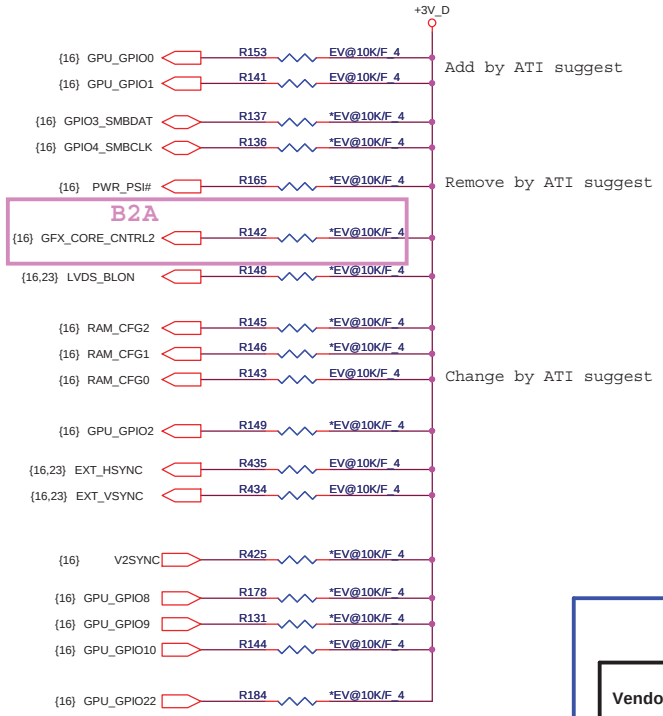
PIN STRAPS



Memory Aperture size	
RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

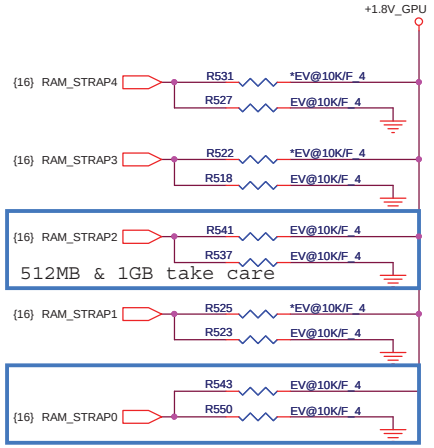
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

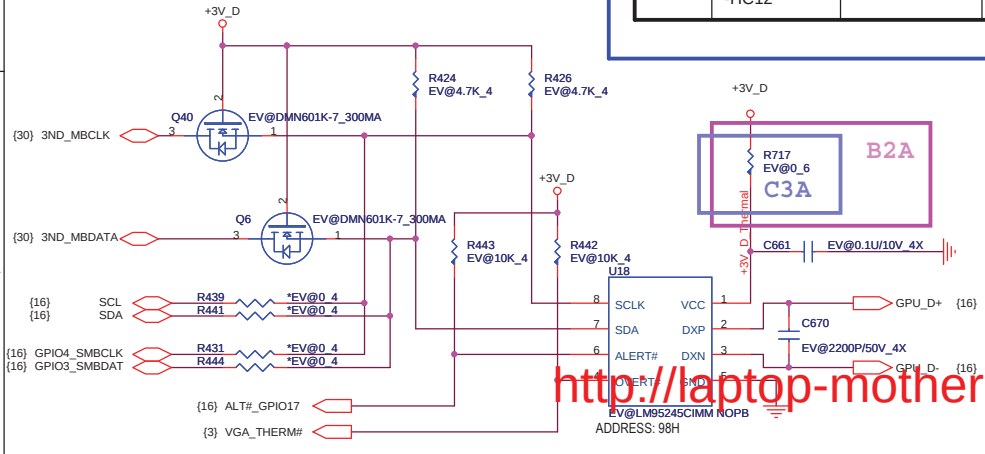
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

DDR3 Memory TYPE

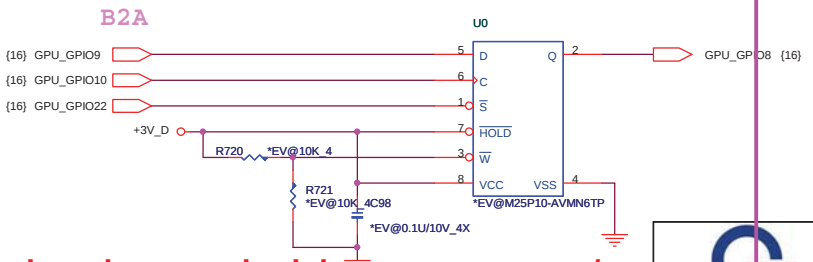
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4 15"	RAM_STRAP4 14"
Hynix	H5TQ1G63BFR -12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
			2GB	0	0	1	0	0	1
Samsung	K4W1G1646E -HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
	K4W2G1646B -HC12	AKD5MGGT501	2GB	0	0	1	1	0	1



Thermal Sensor



EEPROM



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	Memory strip/Thermal/HDCP	A1A
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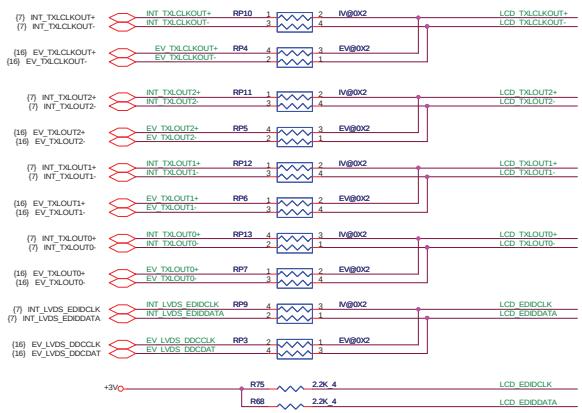
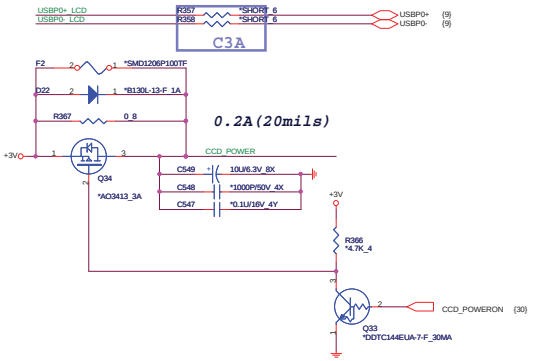
LVDS Signals

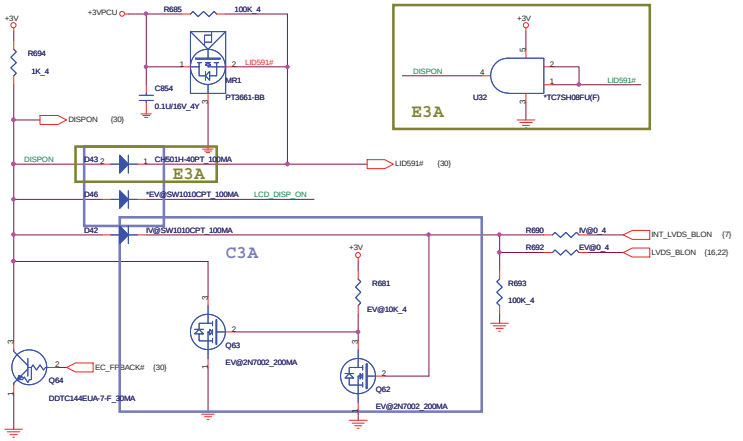


LVDS Enable

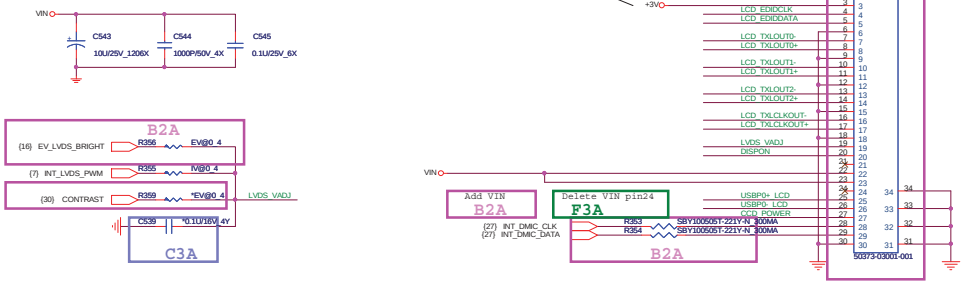
CCD



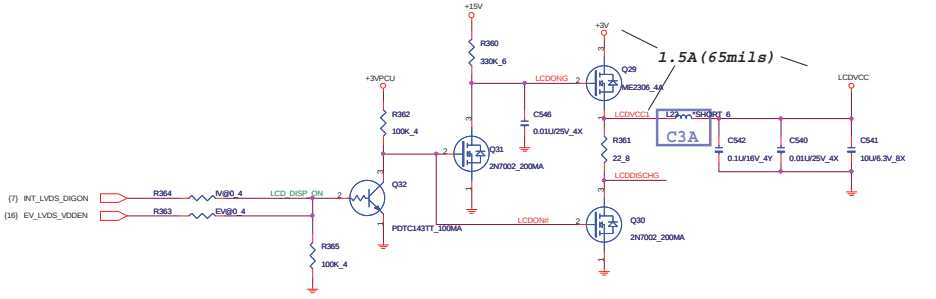
HALL SENSOR&BACK LIGHT SWITCH



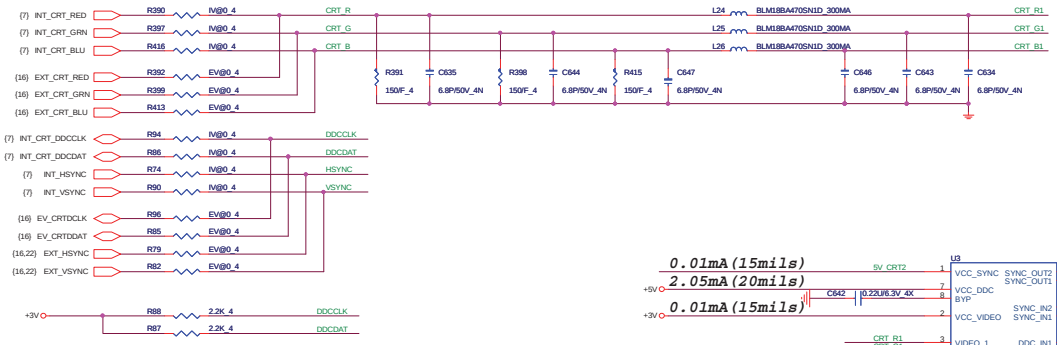
LCD Panel Module

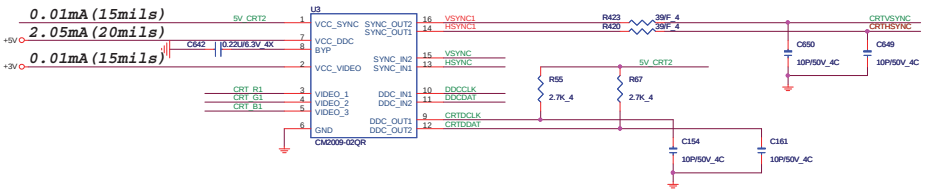


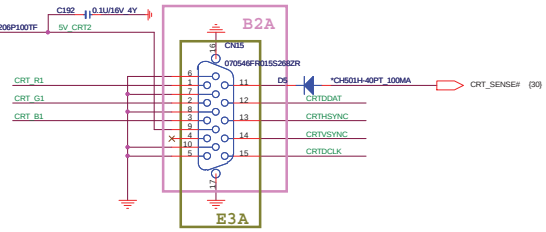
LCD POWER SWITCH

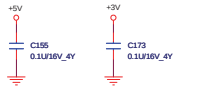


CRT









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Size	Document Number	Rev
	LCD/LED Panel/CCD	A1A
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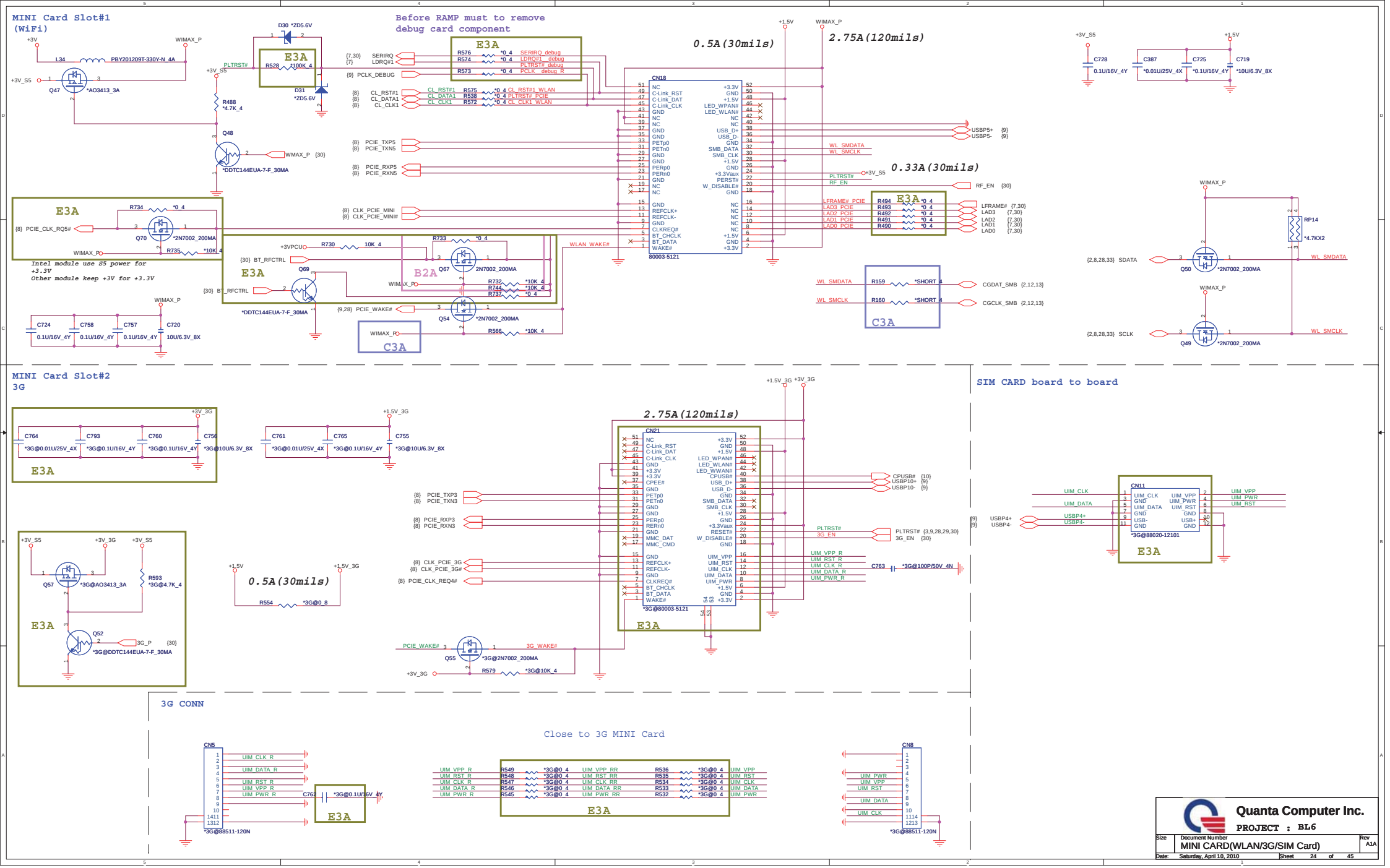

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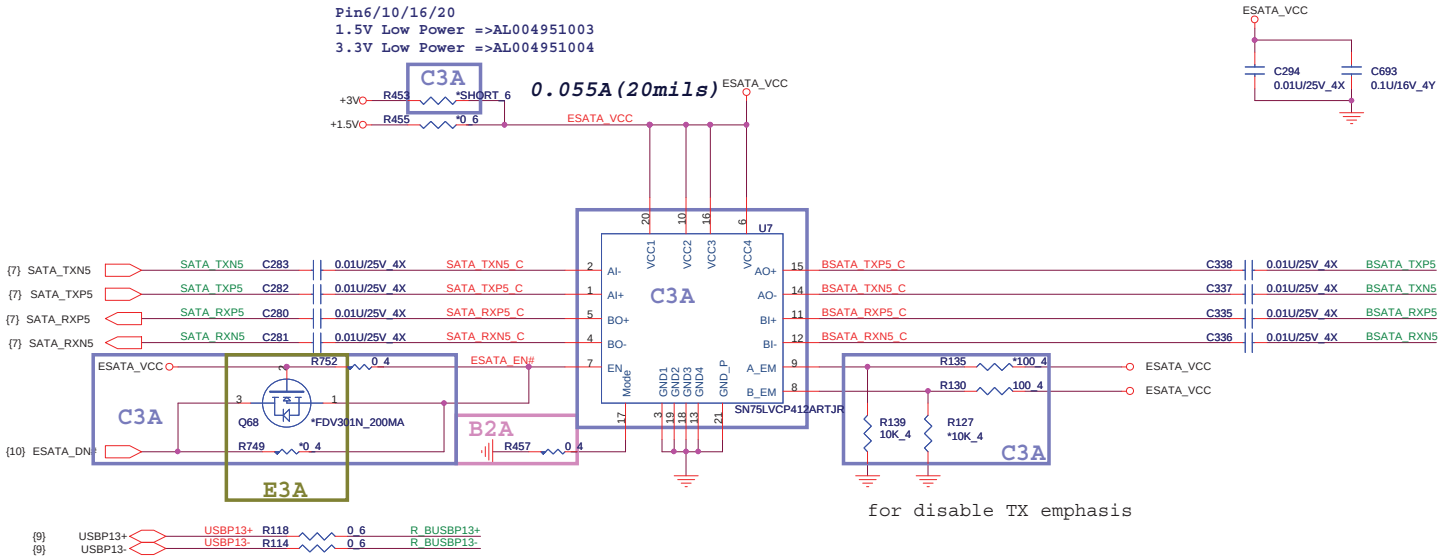
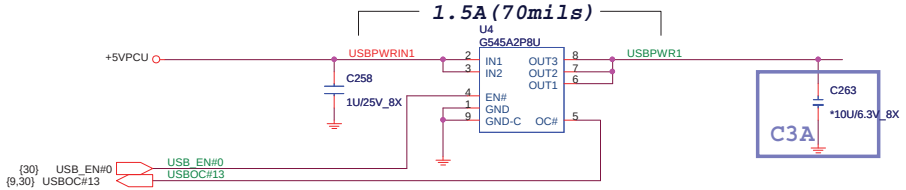
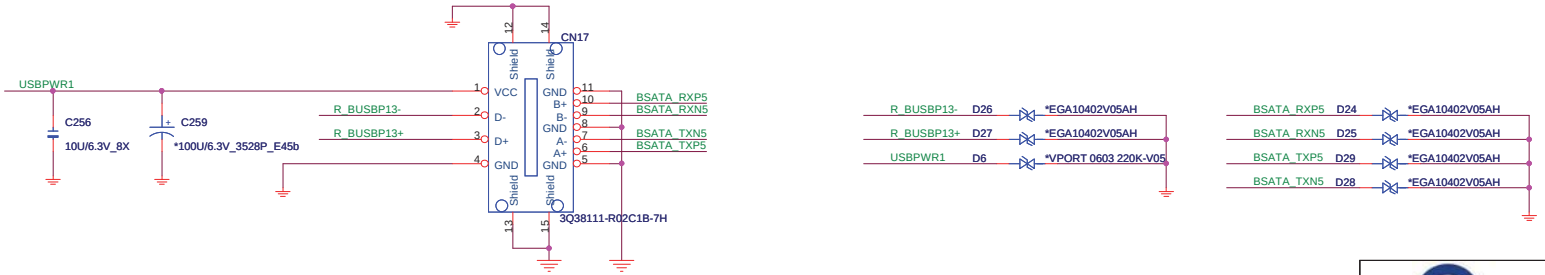
ESATA Re-driver IC





ESATA CONN



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	TP/SW/ESATA/USB+Audio/LED	A1A
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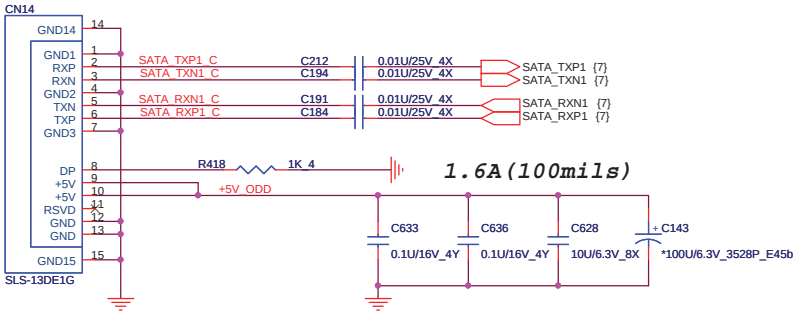
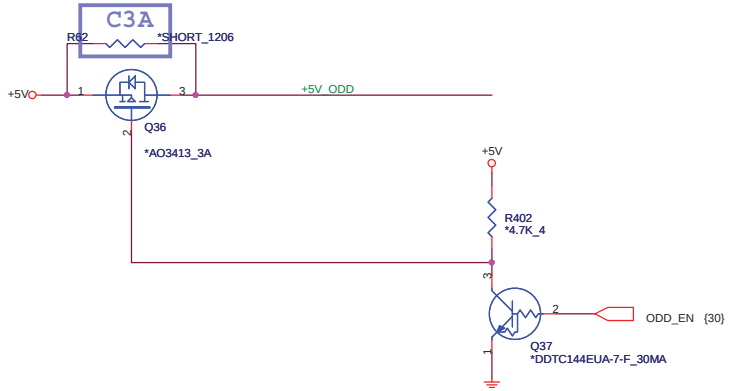
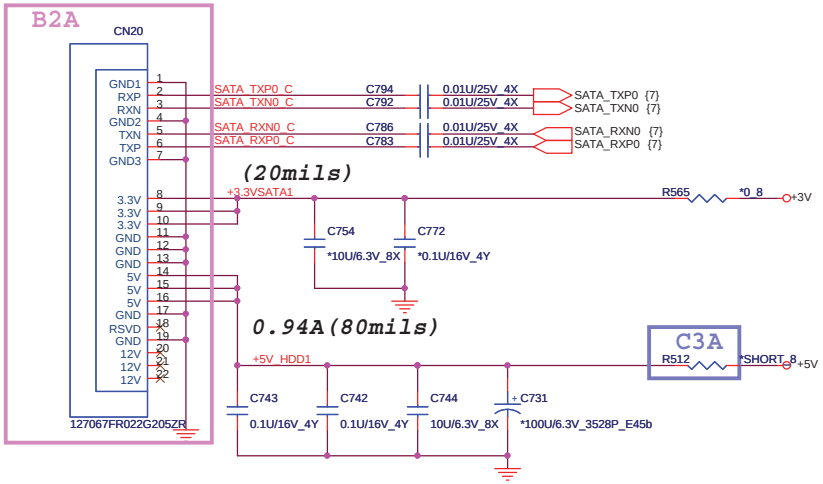
SATA ODD

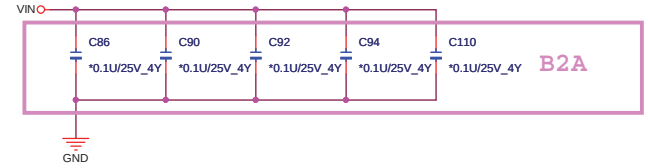


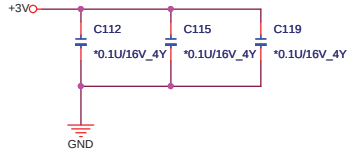


SATA HDD



EMI





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Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	HDD/ODD/EMI	A1A
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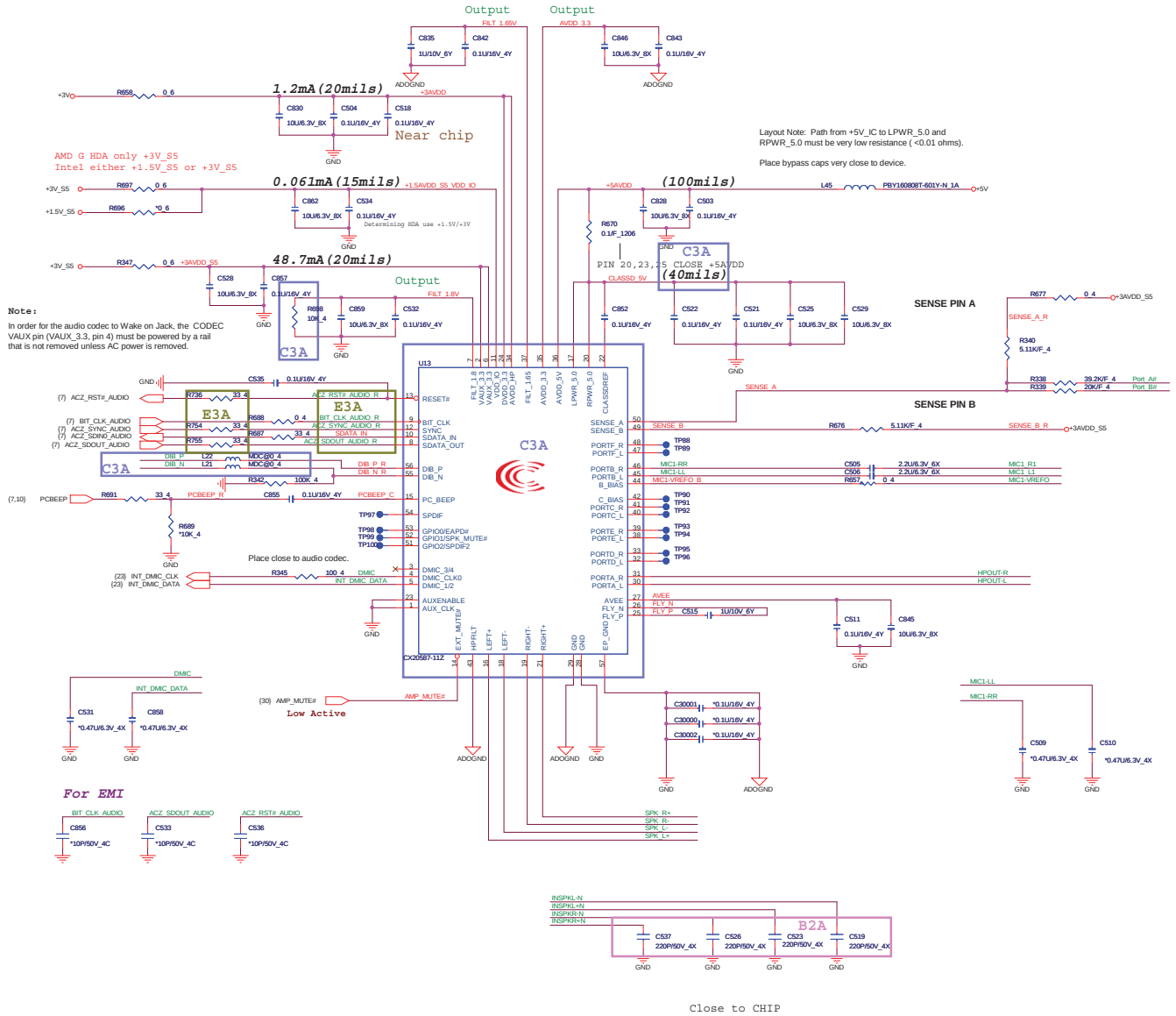
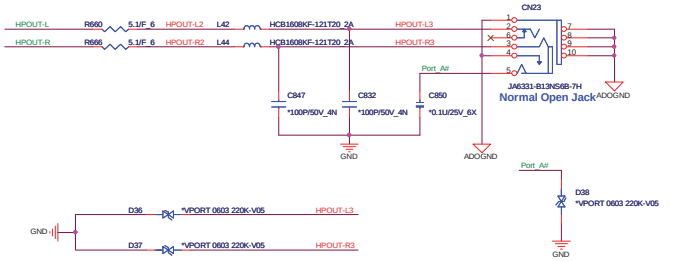
Codec (CX20587)

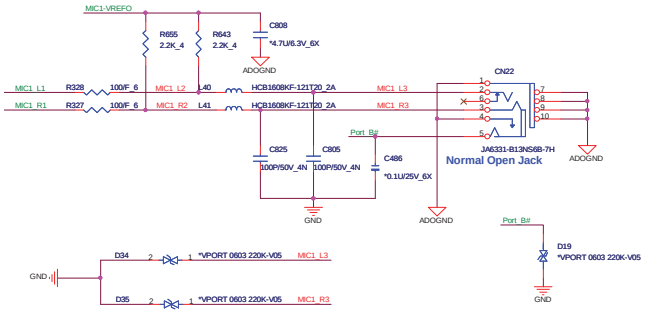


AUDIO JACKS

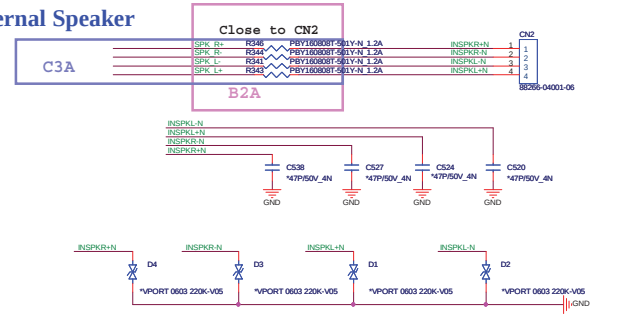
Earphone



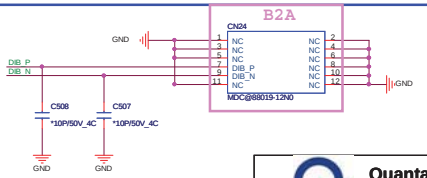
External MIC



Internal Speaker



MDC



Quanta Computer Inc.		
PROJECT : BL6		
Size	Document Number: Audio Codec (CX20583)	Rev: A1A
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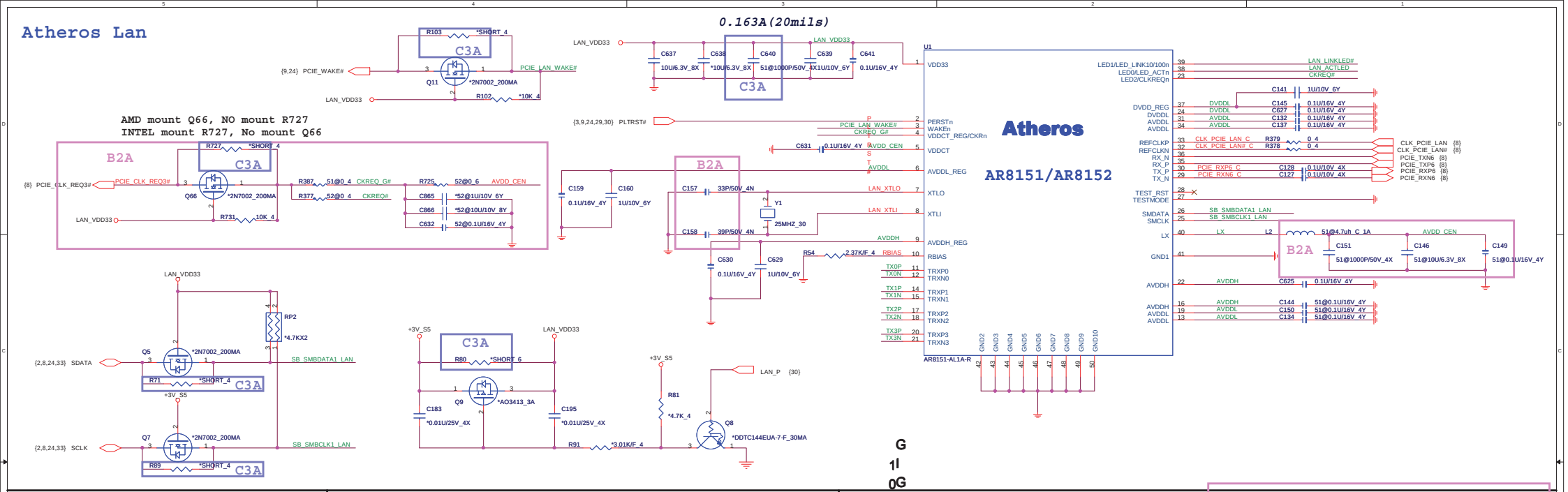
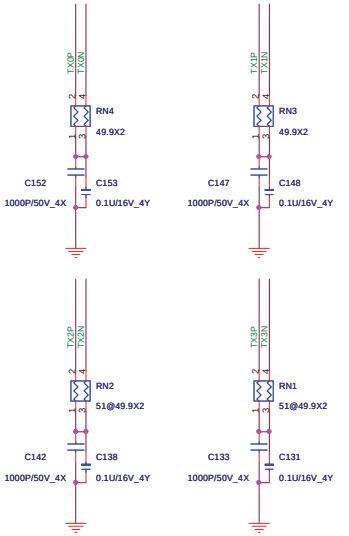
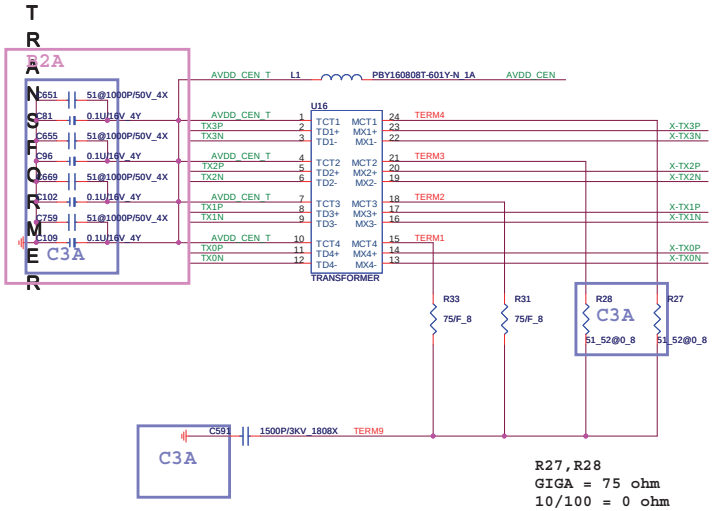
Atheros Lan



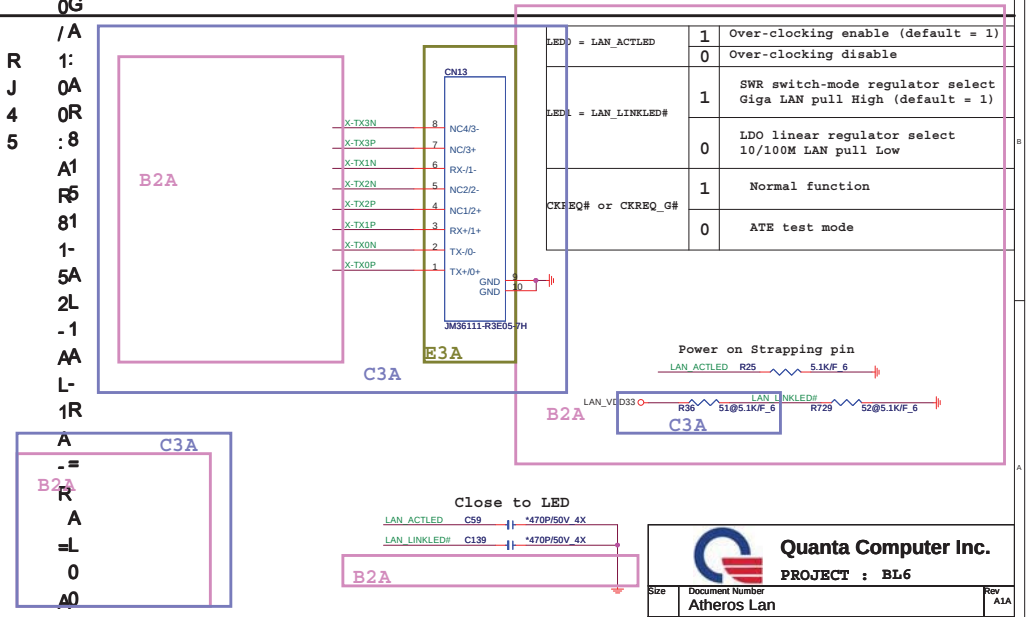
PLACE NEAR LAN IC SIDE



TRANSFORMER



RJ45



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Size | Document Number: Atheros Lan | Rev: A1A
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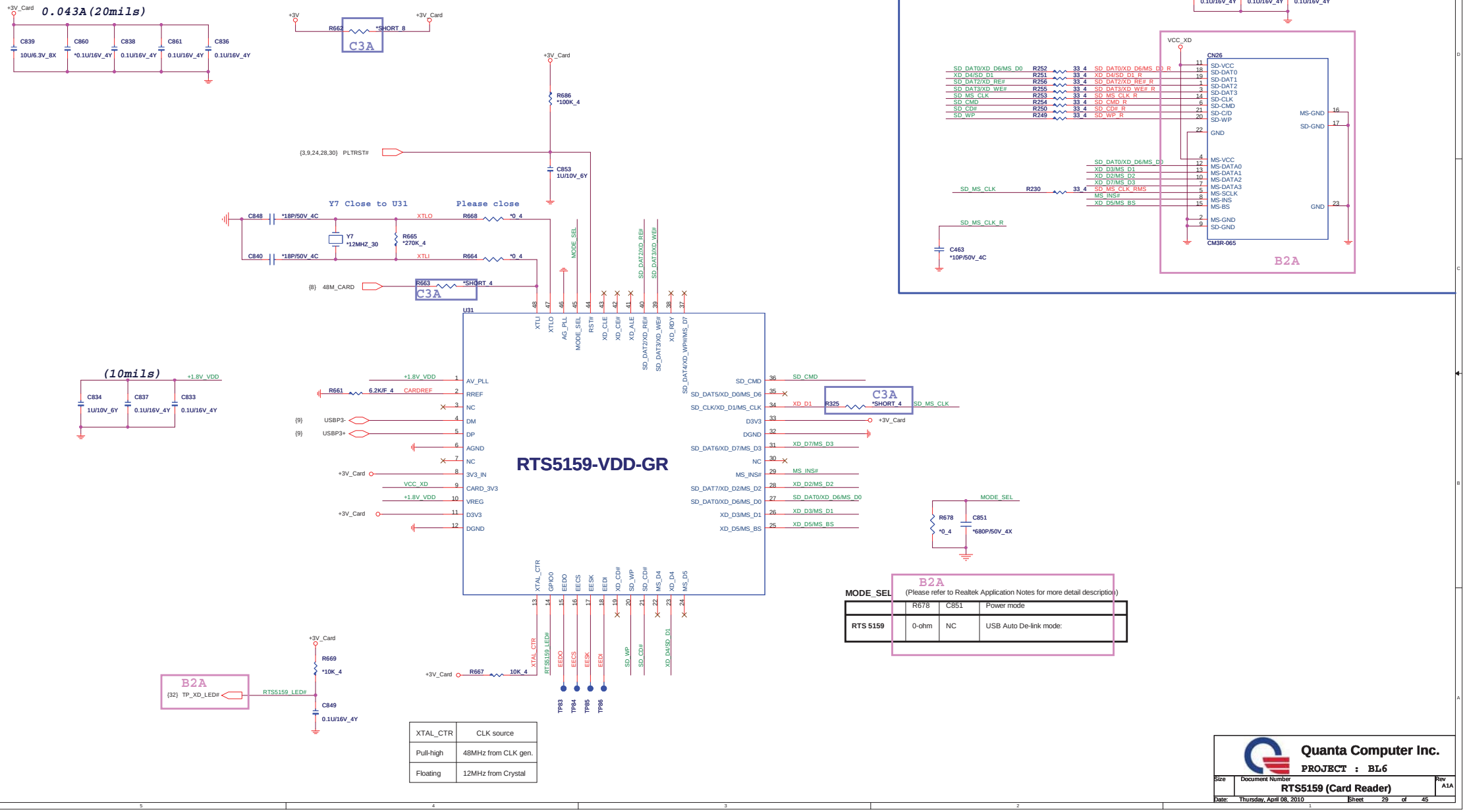
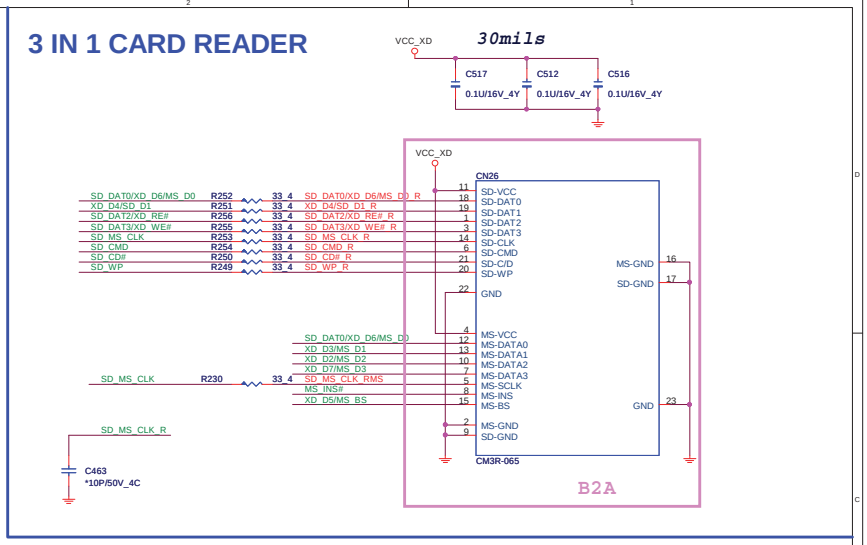
5 IN 1 CARD READER



MODE_SEL	B2A (Please refer to Realtek Application Notes for more detail description)		
	R678	C851	Power mode
RTS 5159	0-ohm	NC	USB Auto De-link mode:

XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

3 IN 1 CARD READER



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Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	RTS5159 (Card Reader)	A1A

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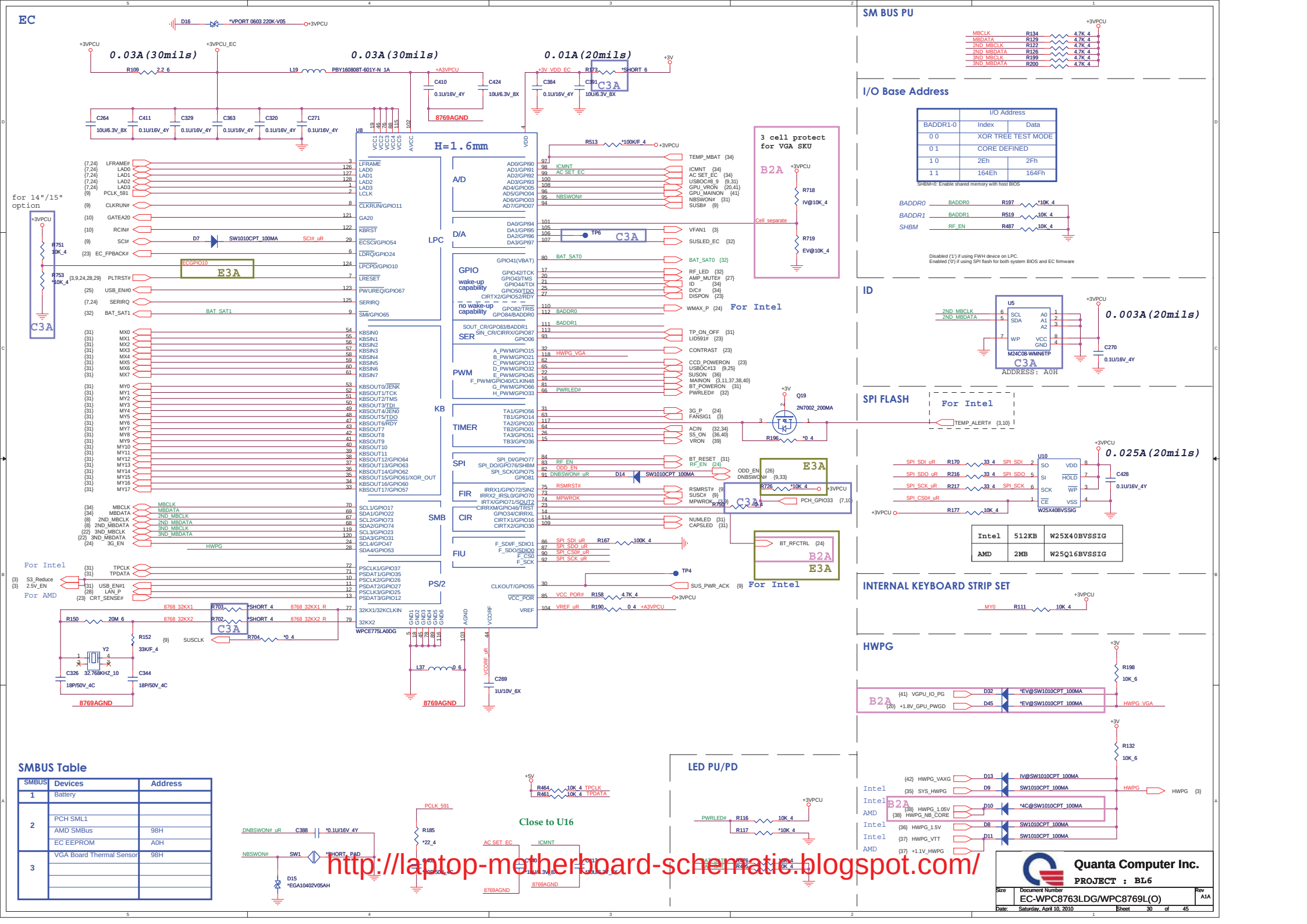

SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	AMD SMBus	98H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

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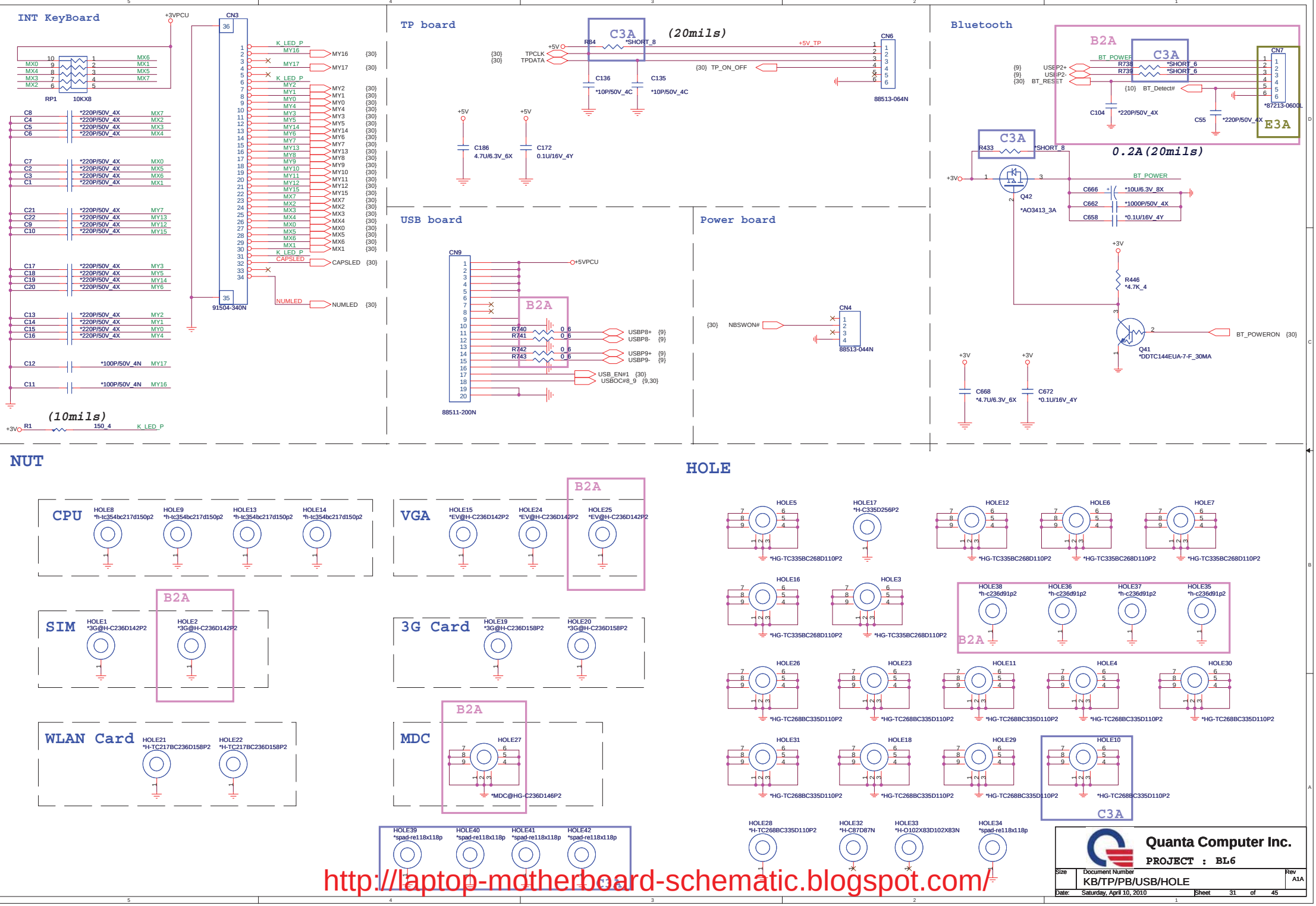
INT KeyBoard
TP board
Bluetooth
USB board
Power board
NUT
HOLE
CPU
VGA
SIM
3G Card
WLAN Card
MDC
Quanta Computer Inc.
PROJECT : BL6
KB/TP/PB/USB/HOLE
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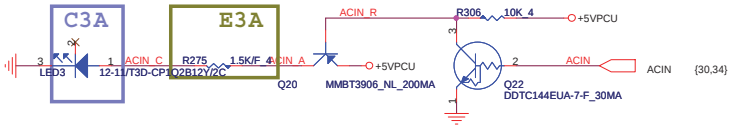
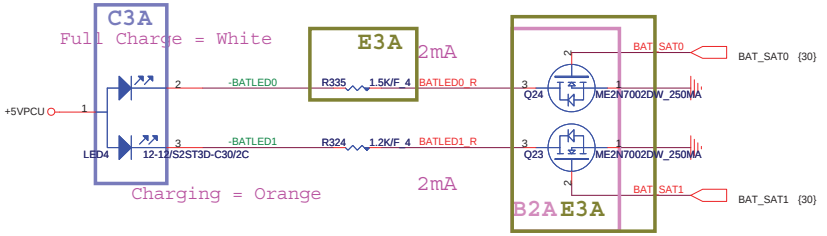
LED

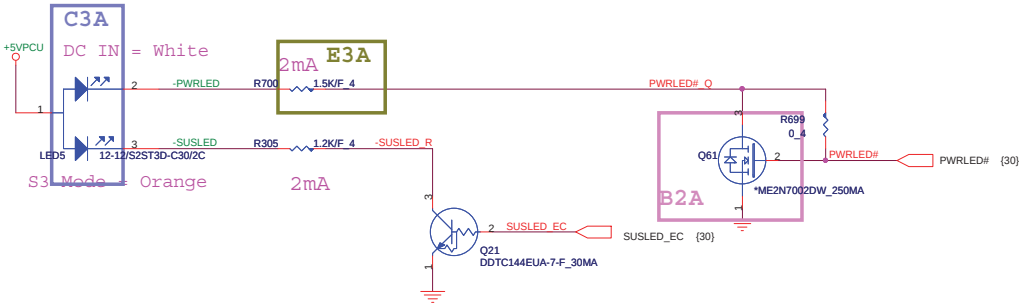
AC-IN



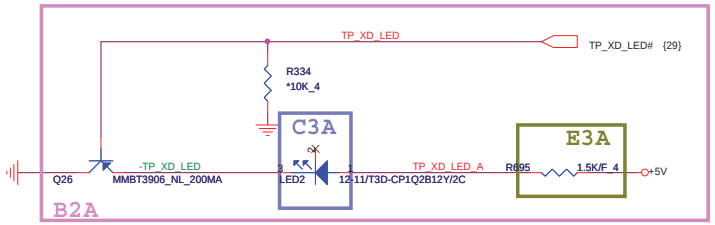
BATERRY



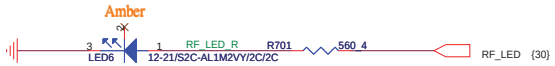
POWER



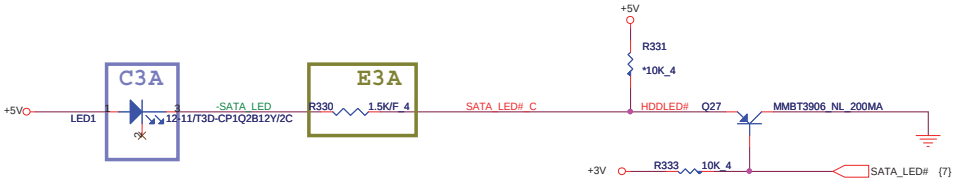
CARDREADER



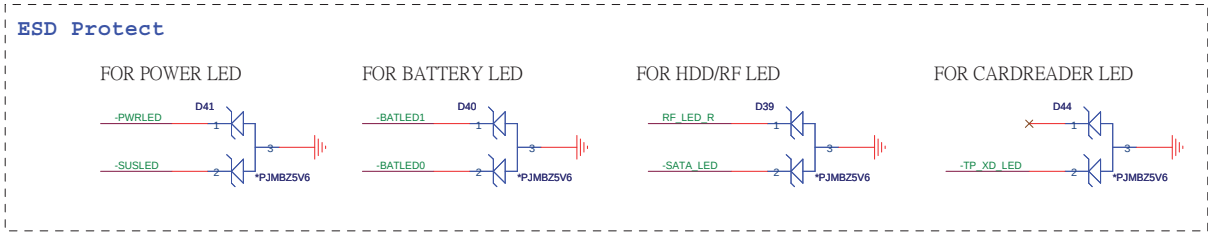
RF LED



HDD/ODD



ESD Protect



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Quanta Computer Inc.
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Size	Document Number	Rev
	LED	A1A

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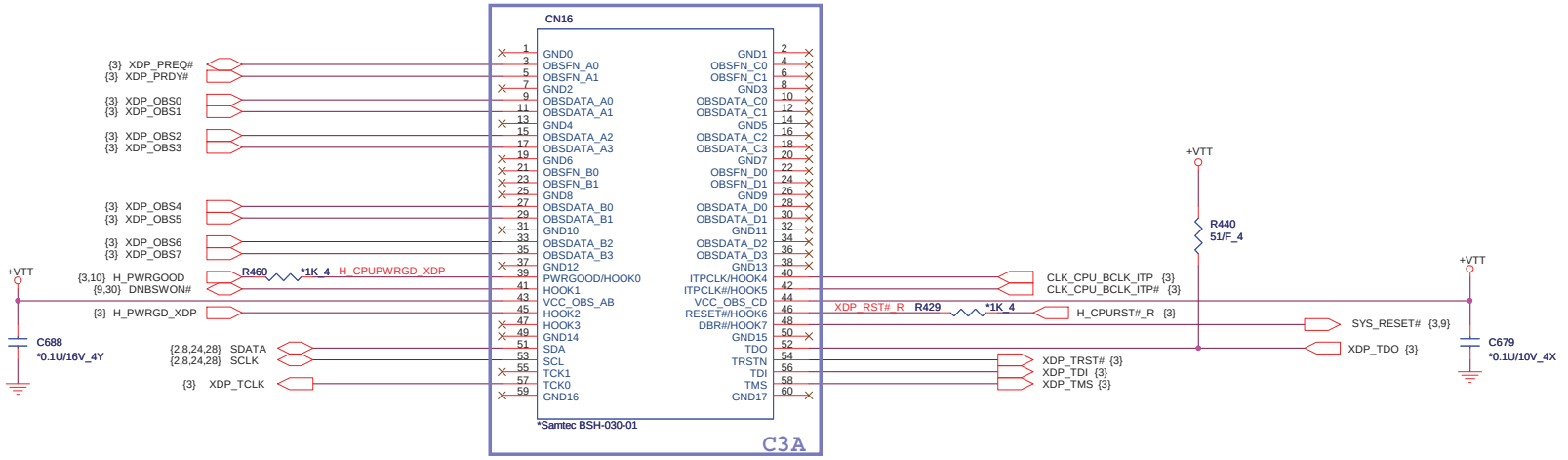
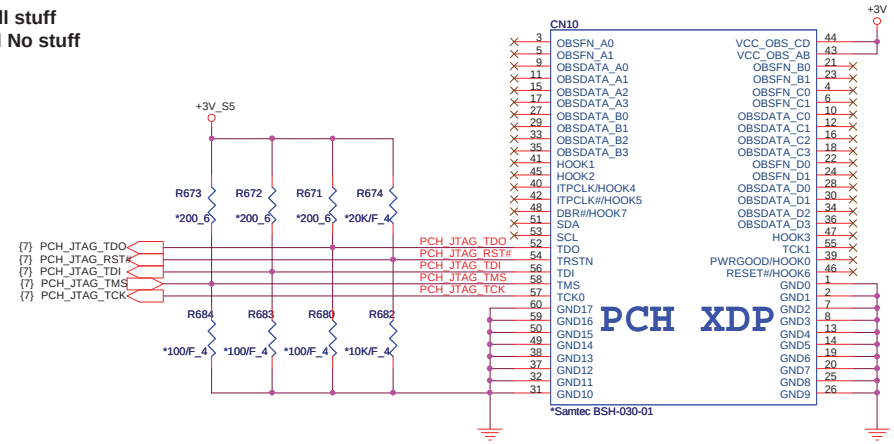
CPU XDP



Feature Set	SKU Name (S)				
	Q57	H57	H55	P55	P57
BraidWood	Y	Y	N	N	Y

PCH XDP

Note: For ES1/ES2 version all stuff
Production version all No stuff



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Quanta Computer Inc.
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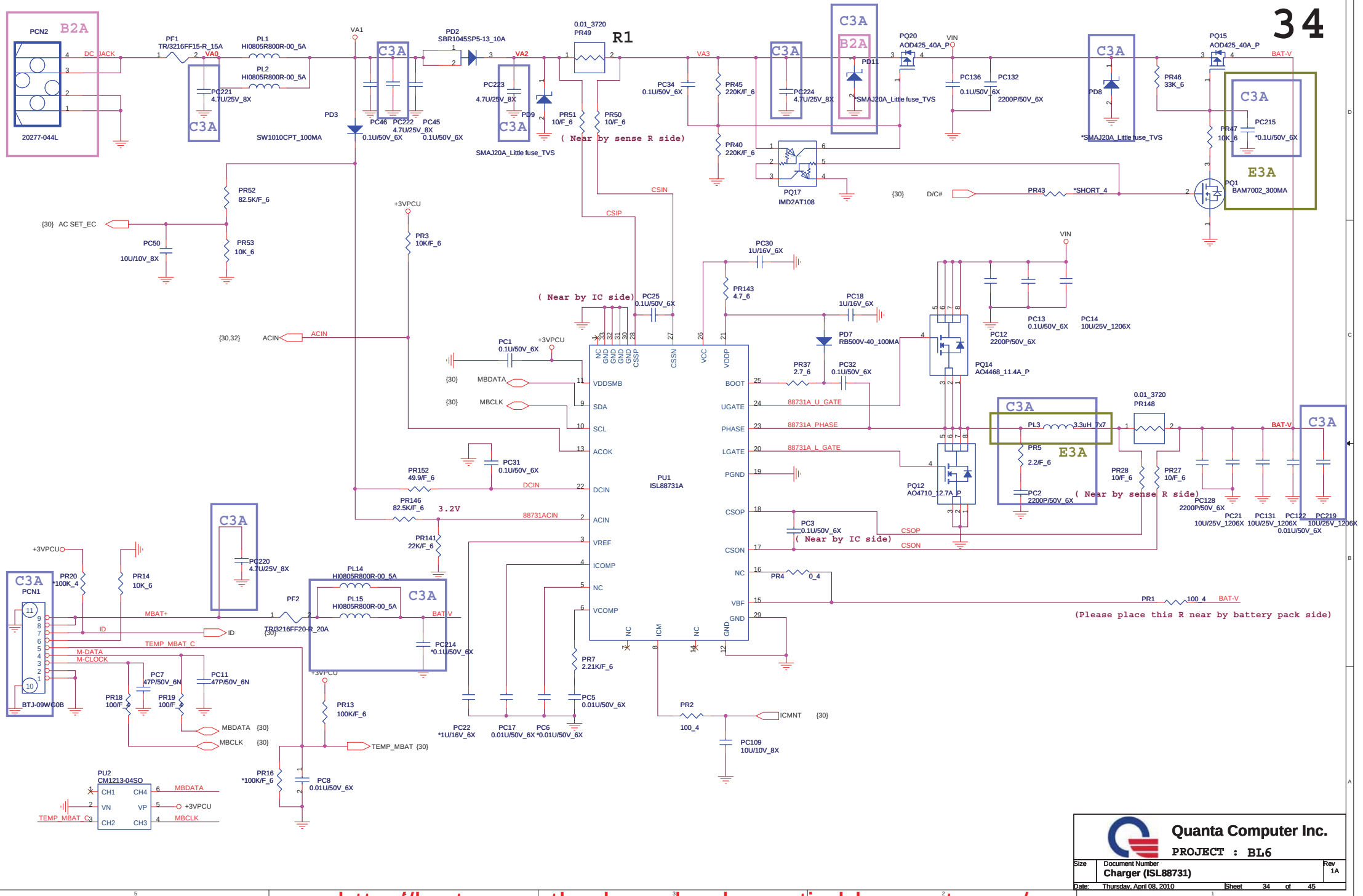
Size	Document Number	Rev
	NVRAM Connector	A1A
Date: Wednesday, April 07, 2010	Sheet 33 of 45	



Quanta Computer Inc.		
PROJECT : BL6		
Size	Document Number: Charger (ISL88731)	Rev: 1A
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MAIND {5,36,40}

For RT8210B 0_4 & 10K_4
For ISL6237 ZD5.6V , 100K/F_4 & 200K/F_4

{3,16} SYS_SHDN# PR91 0_4 39K/F_4 PR92 VL

VIN

(Peak 10.2 ,AVG 8.135A)
f : 400k Hz
OCP:11A

PC92 0.1U/50V_6X PC91 2200P/50V_6X PC93 10U/25V_1206X

*SHORT_4 PR89 *SHORT_4 PR95

PD6 *ZD5.6V PR69 0_4 PR72 10K/F_4 PR78 *200K/F_4

PC85 0.1U/50V_6X PC81 *1U/10V_4X PC88 4.7U/25V_8X PR81 0_4 PC72 0.1U/50V_6X PC76 1U/16V_6X PR76 0_4 PR73 *0_6 REF

PU5 RT8210B

PR90 280K/F_6 PR71 287K/F_6 REFIN2

PC89 0.1U/50V_6X PR84 1/F_6 PC70 0.1U/50V_6X PR79 1/F_6

PQ33 AO4468_11.4A_P PQ32 AO4710_12.7A_P

PR93 *0_6 PR86 0_6 PC99 0.1U/50V_6X PC225 10U/10V_8X PC163 330U/6.3V_105CE_f

PL10 2.2uH_10x10 PR87 2.2/F_6 PC90 2200P/50V_6X

PQ29 AO4468_11.4A_P PQ30 AO4710_12.7A_P

PL8 2.2uH_10x10 PR80 2.2/F_6 PC73 2200P/50V_6X

PR67 0_6 PR68 *0_6

PC64 0.1U/50V_6X PC145 330U/6.3V_105CE_ PC226 10U/10V_8X

f : 500k Hz
(Peak 9A, AVG 7.623A)
OCP:11A

PC71 0.1U/50V_6X PC69 2200P/50V_4X PC74 10U/25V_1206X

PD5 CHN21UPT_100MA PD4 CHN21UPT_100MA PC68 0.1U/50V_6X PC65 0.1U/50V_6X PC67 0.1U/50V_6X PR66 22_8 PC66 0.1U/50V_6X

PC83 1U/16V_6X PR82 0_6 PR70 0_6

PR74 0_6 PR75 *0_6 PR88 *SHORT_4 PR94 10K/F_6

PQ3 AO4496_10A PQ2 AO6402A_7A

PQ4 AO4496_10A PQ59 AO6402A_7A

1.984A
2.744A~4.984A
0.001A
4.253A

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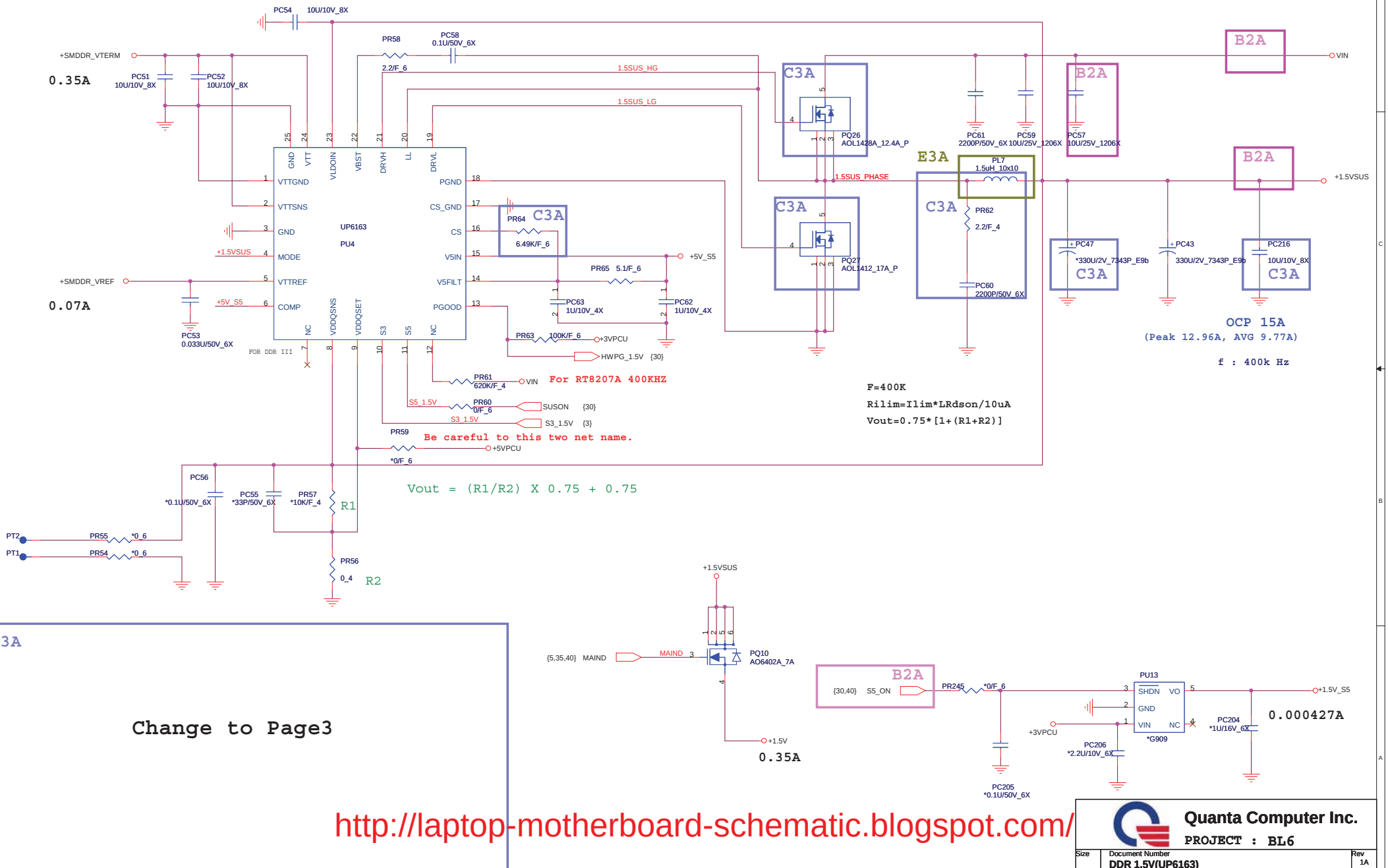
Quanta Computer Inc.
PROJECT : BL6
Size | Document Number: System 5V/3V (ISL6237) | Rev 1A
Date: Wednesday, April 07, 2010 | Sheet 35 of 45



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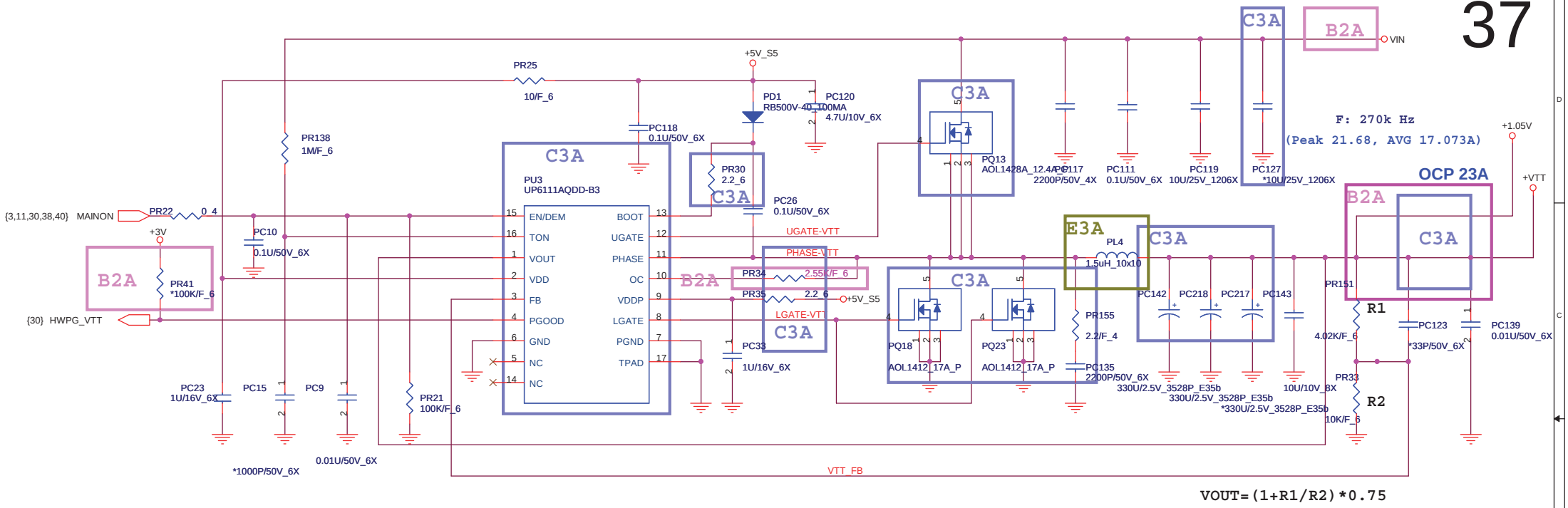
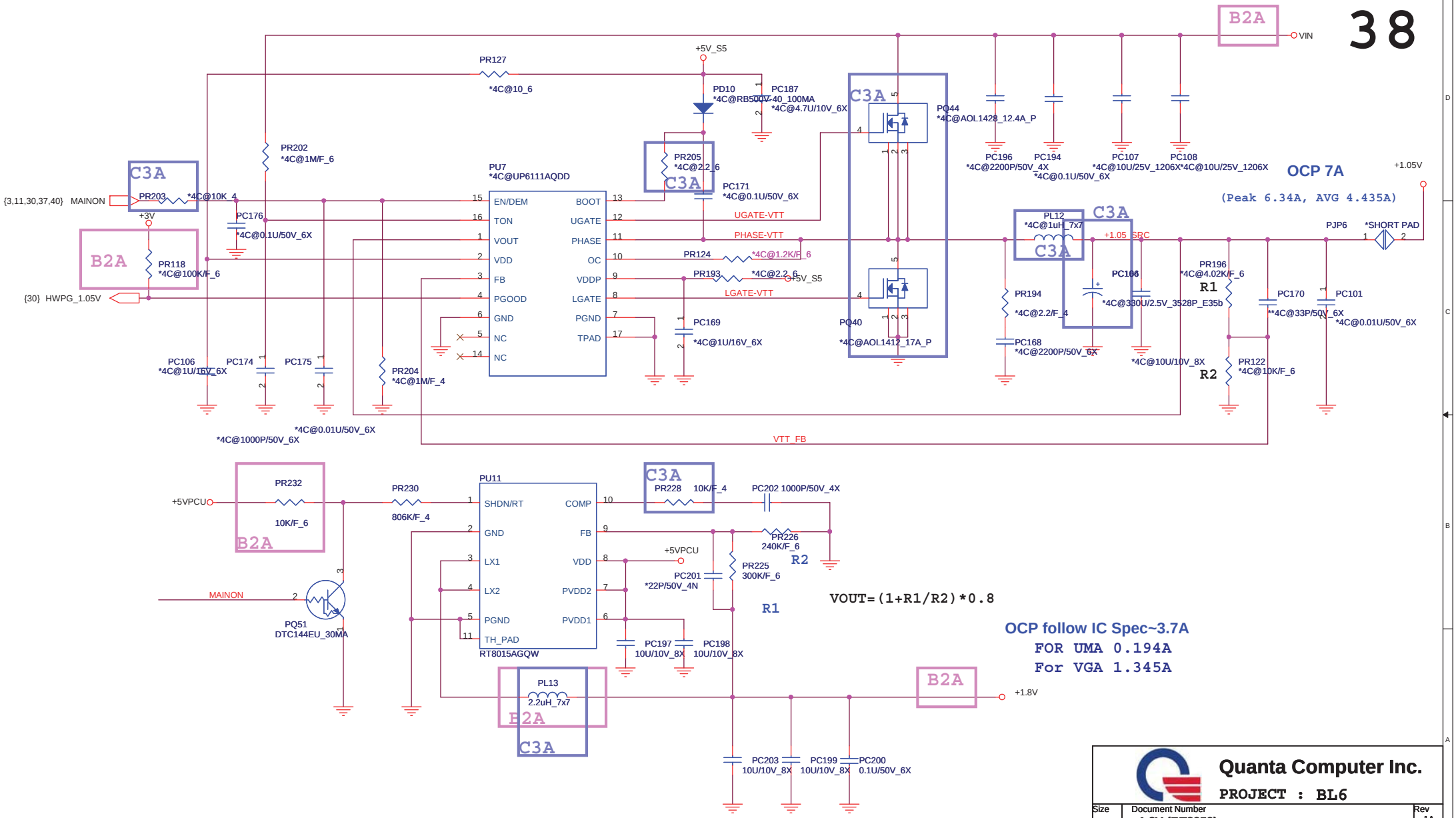
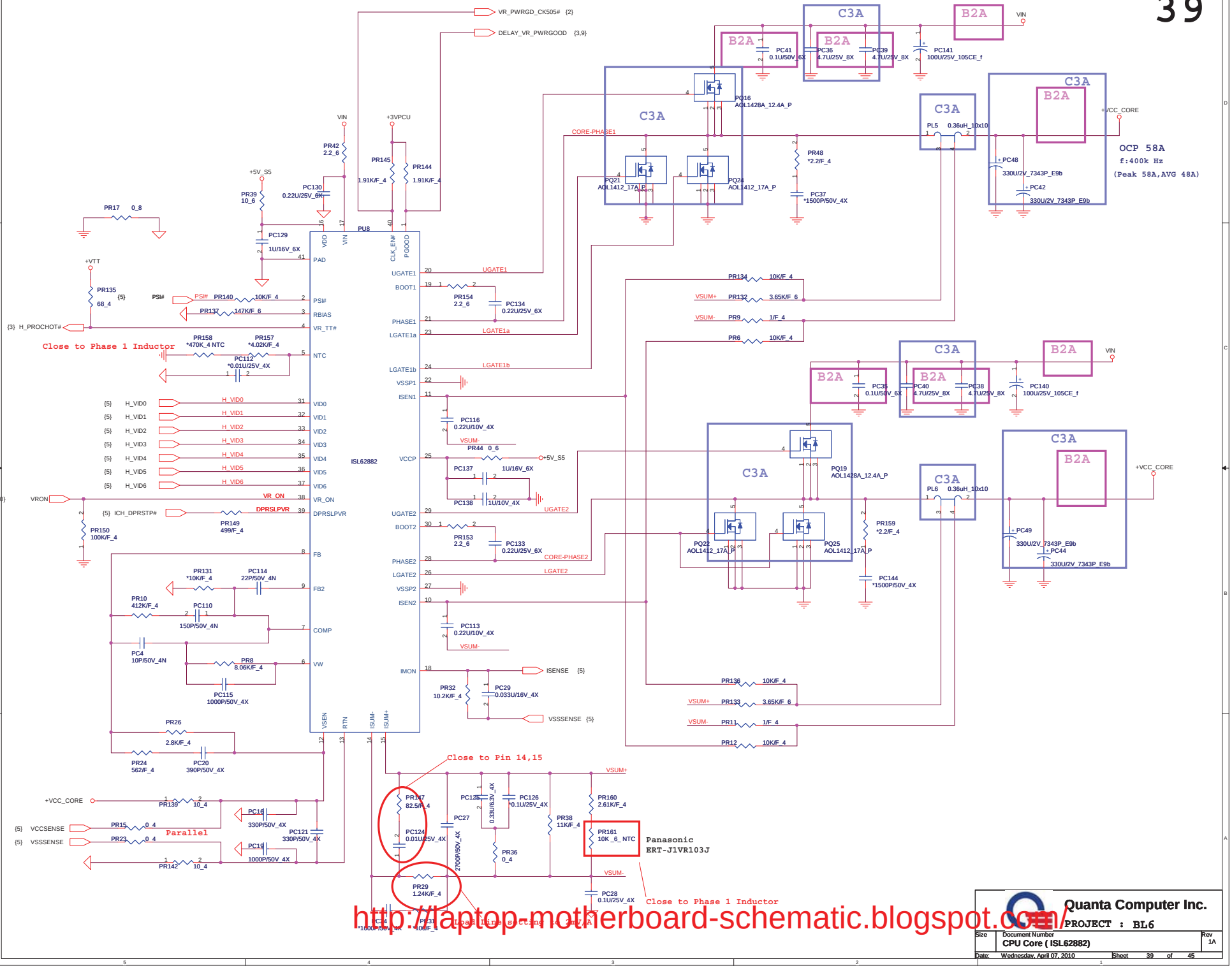
Quanta Computer Inc.	PROJECT : BL6	
Size	Document Number: DDR 1.5V(UP6163)	Rev: 1A
Date: Wednesday, April 07, 2010	Sheet 36 of 45	



http://laptop-motherboard-schematic.blogspot.com/



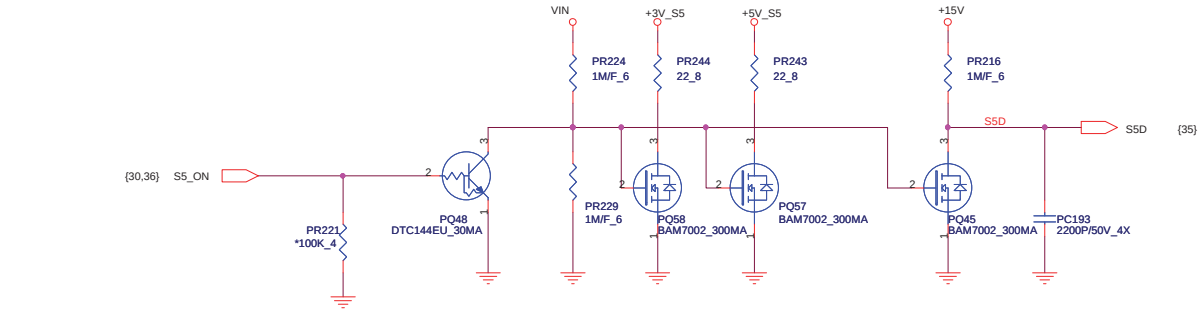
http://laptop-motherboard-schematic.blogspot.com/

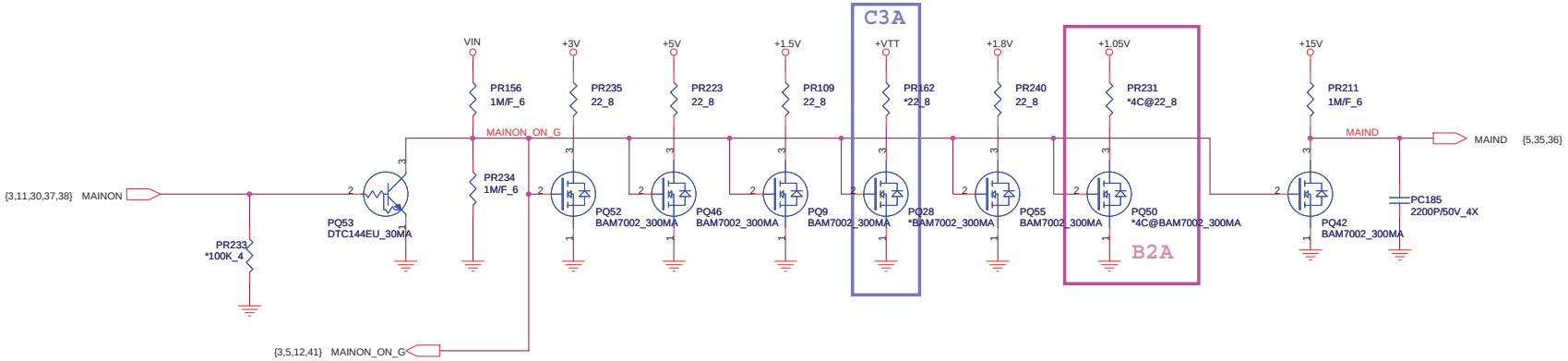


http://laptop-motherboard-schematic.blogspot.com/

Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	CPU Core (ISL62882)	1A
Date: Wednesday, April 07, 2010	Sheet 39 of 45	





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Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	Discharge (1.5V_S5/1.8V)	1A

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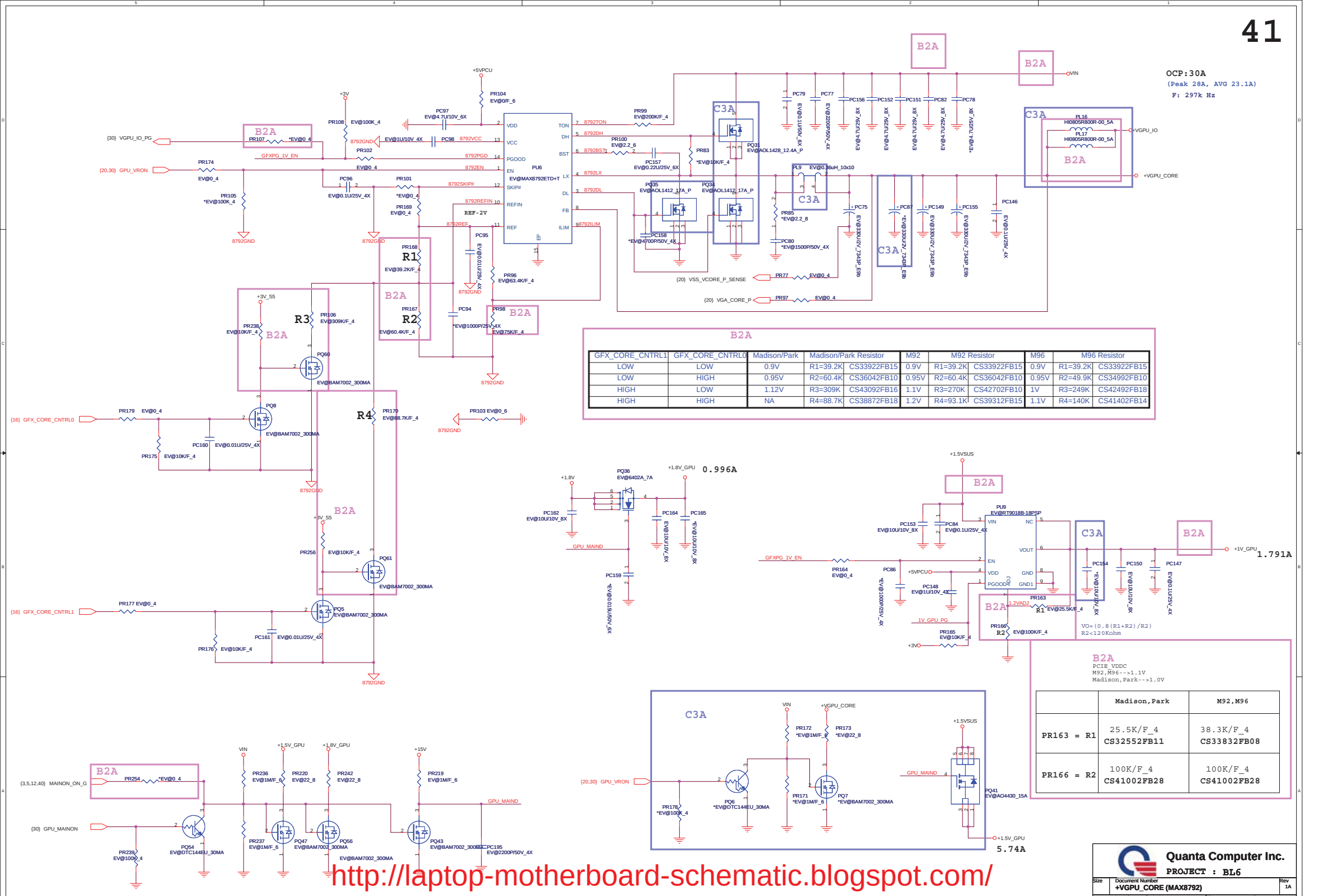

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	Madison/Park	Madison/Park Resistor		M92	M92 Resistor		M96	M96 Resistor	
LOW	LOW	0.9V	R1=39.2K	CS33922FB15	0.9V	R1=39.2K	CS33922FB15	0.9V	R1=39.2K	CS33922FB15
LOW	HIGH	0.95V	R2=60.4K	CS36042FB10	0.95V	R2=60.4K	CS36042FB10	0.95V	R2=49.9K	CS34992FB10
HIGH	LOW	1.12V	R3=309K	CS43092FB16	1.1V	R3=270K	CS42702FB10	1V	R3=249K	CS42492FB18
HIGH	HIGH	NA	R4=88.7K	CS38872FB18	1.2V	R4=93.1K	CS39312FB15	1.1V	R4=140K	CS41402FB14

B2A
PCIE_VDDC
M92,M96-->1.1V
Madison,Park-->1.0V

	Madison,Park	M92,M96
PR163 = R1	25.5K/F_4 CS32552FB11	38.3K/F_4 CS33832FB08
PR166 = R2	100K/F_4 CS41002FB28	100K/F_4 CS41002FB28

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Quanta Computer Inc.
PROJECT : BL6
Size | Document Number: +VGPU_CORE (MAX8792) | Rev 1A
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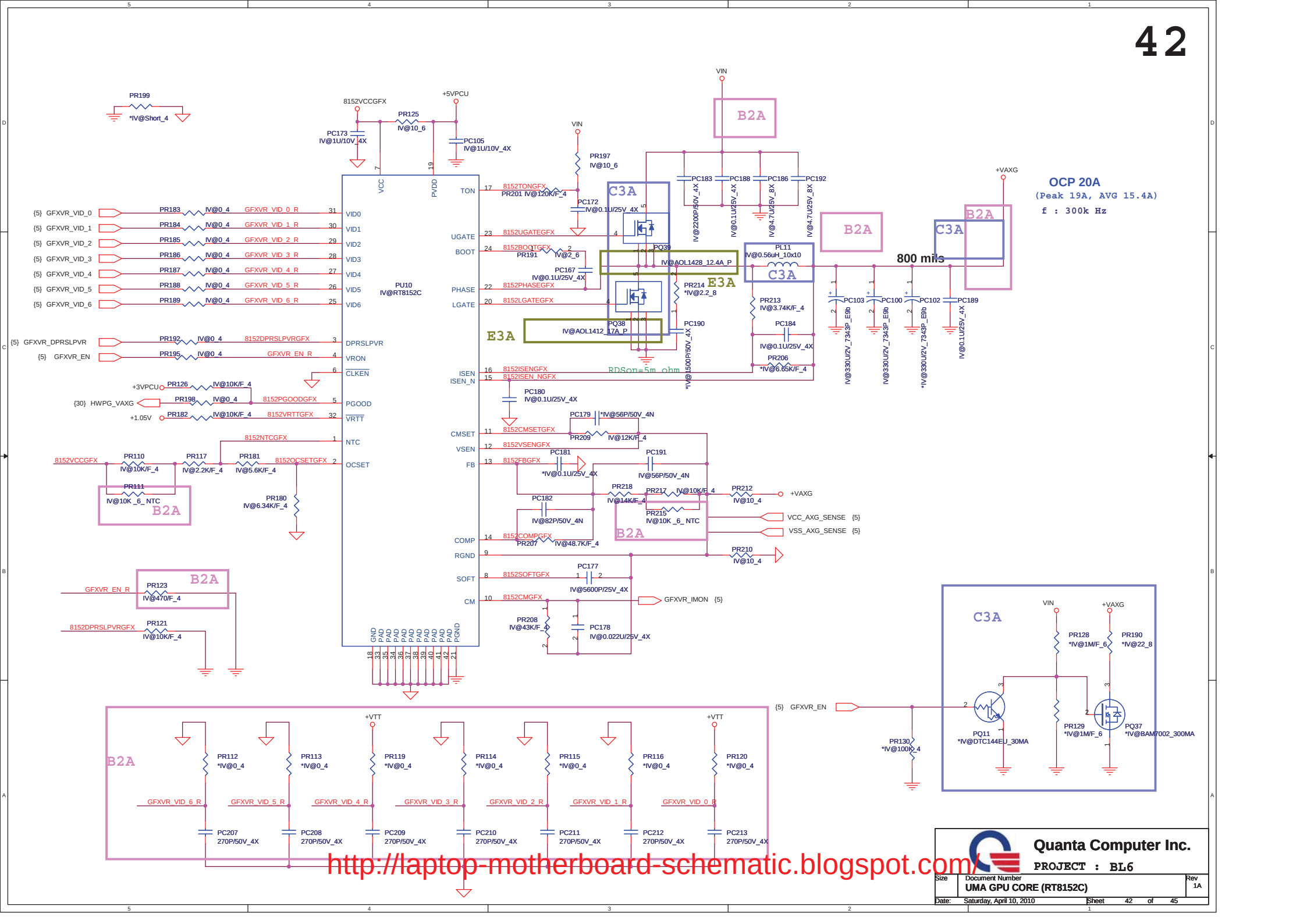

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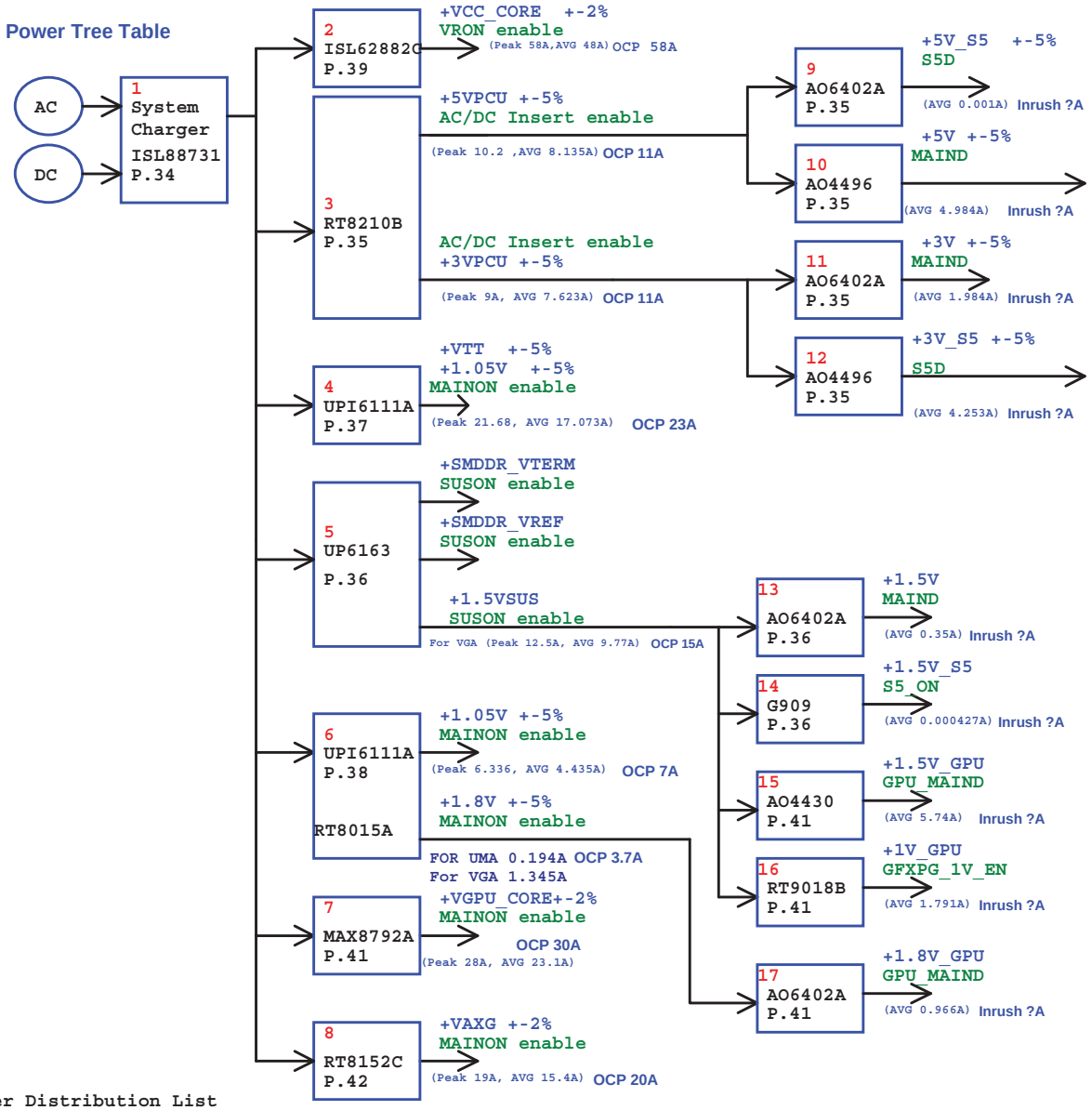
Power Tree Table



Power Distribution List

Power	Distribution

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